



Introduction:

The purpose of this document is to do the post layout SI analysis and verification of load board that is designed for Verigy 93K tester. The board has been designed to test two DUT's, each has 425 ball pins. The chip has interfaces like PCI, PCIE, GPIO and USB. In this analysis, single ended signals and PCIe signals have been verified, to see, if it meets the spec. Post layout SI verification has been carried out to verify the following.

- Impedance Matching
- Return & Insertion Loss Analysis
- Crosstalk Analysis (NEXT & FEXT)
- DC/AC Resistance Analysis
- Propagation Delay Matching (skew)
- Analysis of Coupled Differential pairs.
- Interconnect Bandwidth Verification

Tools used:

1. Allegro PCB SI
2. Allegro SigXplorer

Stack up:

The board has hybrid stackup that uses both Rogers 4350 material and Nelco 4000-13 material. High speed signals like PCIe, USB are constrained to route with the Roger Dielectric. Low speed signals are routed with the Nelco 4000-13 dielectrics. This kind of hybrid stackup provides advantage of using low dielectric constant, low loss tangent material for high speed signal and also keeping the board cost to minimum by using low cost dielectric for low speed signal.

Stackup has been designed for 50 Ohm Single ended impedance. The board thickness is around 160 mils. The layer span is 28 layers with 6 digital layers and 3 analog signal layer. The trace width and the dielectric height to achieve the required impedance are shown below:

Subclass Name	Type	Material	Thickness (MIL)	Conductivity (nho/cm)	Dielectric Constant	Loss Tangent	Negative Airwork	Shield	Width (MIL)	Impedance (ohm)
	SURFACE	AIR								
TOP	CONDUCTOR	COPPER	1.4	595900	3.800000	0.008			9.000	52.489
	DIELECTRIC	NELCO_4000_13	5	0	3.800000	0.008				
DGND1	PLANE	COPPER	0.7	595900	3.800000	0.008				
	DIELECTRIC	ROGERS_4350	8	0	3.500000	0.0031				
DSIG1	CONDUCTOR	COPPER	0.7	595900	3.500000	0.0031			8.000	50.432
	DIELECTRIC	ROGERS_4350	8	0	3.500000	0.0031				
DGND2	PLANE	COPPER	0.7	595900	3.800000	0.008				
	DIELECTRIC	NELCO_4000_13	7	0	3.800000	0.008				
DSIG2	CONDUCTOR	COPPER	0.7	595900	3.800000	0.008			6.500	49.889
	DIELECTRIC	NELCO_4000_13	7	0	3.800000	0.008				
DGND3	PLANE	COPPER	0.7	595900	3.800000	0.008				
	DIELECTRIC	NELCO_4000_13	7	0	3.800000	0.008				
DSIG3	CONDUCTOR	COPPER	0.7	595900	3.800000	0.008			6.500	49.889
	DIELECTRIC	NELCO_4000_13	7	0	3.800000	0.008				
DGND4	PLANE	COPPER	0.7	595900	3.800000	0.008				
	DIELECTRIC	NELCO_4000_13	7	0	3.800000	0.008				
DSIG4	CONDUCTOR	COPPER	0.7	595900	3.800000	0.008			6.500	49.889
	DIELECTRIC	NELCO_4000_13	7	0	3.800000	0.008				
DGND5	PLANE	COPPER	0.7	595900	3.800000	0.008				
	DIELECTRIC	NELCO_4000_13	7	0	3.800000	0.008				
DSIG5	CONDUCTOR	COPPER	0.7	595900	3.800000	0.008			6.500	49.889
	DIELECTRIC	NELCO_4000_13	7	0	3.800000	0.008				
DGND6	PLANE	COPPER	0.7	595900	3.800000	0.008				
	DIELECTRIC	NELCO_4000_13	7	0	3.800000	0.008				
DSIG6	CONDUCTOR	COPPER	0.7	595900	3.800000	0.008			6.500	49.889
	DIELECTRIC	NELCO_4000_13	7	0	3.800000	0.008				
DGND7	PLANE	COPPER	1.35	595900	3.800000	0.008				
	DIELECTRIC	NELCO_4000_13	5	0	3.800000	0.008				
POWER_1	PLANE	COPPER	1.35	595900	3.800000	0.008				
	DIELECTRIC	NELCO_4000_13	5	0	3.800000	0.008				
POWER_2	PLANE	COPPER	1.35	595900	3.800000	0.008				
	DIELECTRIC	NELCO_4000_13	5	0	3.800000	0.008				
POWER_3	PLANE	COPPER	1.35	595900	3.800000	0.008				
	DIELECTRIC	NELCO_4000_13	5	0	3.800000	0.008				
POWER_4	PLANE	COPPER	1.35	595900	3.800000	0.008				
	DIELECTRIC	NELCO_4000_13	5	0	3.800000	0.008				
POWER_5	PLANE	COPPER	1.35	595900	3.800000	0.008				
	DIELECTRIC	NELCO_4000_13	5	0	3.800000	0.008				
POWER_6	PLANE	COPPER	1.35	595900	3.800000	0.008				
	DIELECTRIC	NELCO_4000_13	5	0	3.800000	0.008				
AGND_1	PLANE	COPPER	0.7	595900	3.800000	0.008				
	DIELECTRIC	NELCO_4000_13	7	0	3.800000	0.008				
ASIG_1	CONDUCTOR	COPPER	0.7	595900	3.800000	0.008			6.500	49.889



Differential signals are designed for 100 ohms differential impedance and trace width and spacing's are controlled as shown below:

Subclass Name	Type	Thickness (MIL)	Dielectric Constant	Loss Tangent	Shield	Width (MIL)	Impedance (ohm)	Coupling Type	Spacing (MIL)	DiffZ0 (ohm)
1	SURFACE									
2	TOP	CONDUCTOR	1.4	3.800000	0.008	9.000		NONE		
3		DIELECTRIC	5	3.800000	0.008					
4	DGND1	PLANE	0.7	3.800000	0.008					
5		DIELECTRIC	8	3.900000	0.0031					
6	DSIG1	CONDUCTOR	0.7	3.500000	0.0031	7.500		EDGE	15.000	101.83
7		DIELECTRIC	8	3.500000	0.0031					
8	DGND2	PLANE	0.7	3.800000	0.008					
9		DIELECTRIC	7	3.800000	0.008					
10	DSIG2	CONDUCTOR	0.7	3.800000	0.008	6.000		EDGE	12.000	100.5
11		DIELECTRIC	7	3.800000	0.008					
12	DGND3	PLANE	0.7	3.800000	0.008					
13		DIELECTRIC	7	3.800000	0.008					
14	DSIG3	CONDUCTOR	0.7	3.800000	0.008	6.000		EDGE	12.000	100.5
15		DIELECTRIC	7	3.800000	0.008					
16	DGND4	PLANE	0.7	3.800000	0.008					

PCIe signals are routed with 7.5 mils trace width and inter-spacing of 15 mils.

Impedance matching:

The reflection analysis is carried out to find any potential impedance discontinuity in the design. Stack up has been finalised in the completed design. Reflection analysis is done and the design is verified for positive noise margin, and Ringing. Dut has been modeled using TDR model and POGO pins are modeled as 50 ohm terminators. Reflection report for the address net taken for DUT 0 is shown below. Positive margins indicate that no significant reflections are present due to impedance mismatch.

Reflection Report

```

*****
# Allegro PCB SI 630 (SPECCTRAQuest)
# 15.51 p006 (v15-5 1-436) [11-15-2005]
#
# (c) Copyright 1998-2004 Cadence Design Systems, Inc.
# Report: Standard Reflection Summary Sorted By Worst Settle Delay
*****

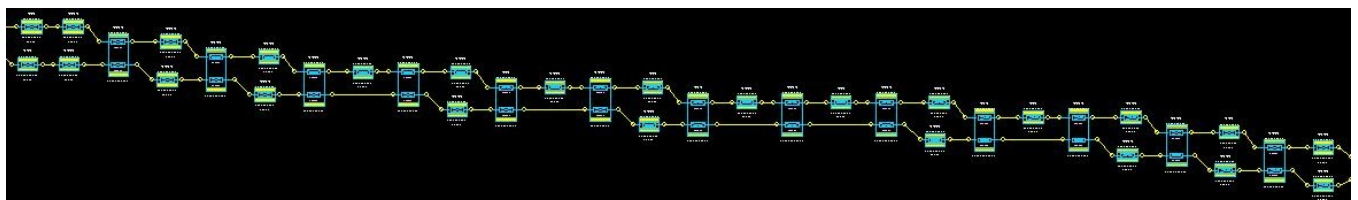
*****
Delays (ns), Distortion (mV), (Typ FTSMode)
*****
XNet      Drvr      Rcvr      NMHigh    NMLow    OShootHigh OShootLow SwitchRise SwitchFall
-----
1 301928-2218 DUT0_MEM_ADD<12> 301928-2218 DUT0 AC9 301928-2218 132 D03 382 9 400 982 9 -0.04714 2.032 2.031
1 301928-2218 DUT0_MEM_ADD<9> 301928-2218 DUT0 V9 301928-2218 130 D02 385 7 399 9 985 8 -0.07035 1.671 1.665
1 301928-2218 DUT0_MEM_ADD<5> 301928-2218 DUT0 V8 301928-2218 129 D02 386 9 399 9 987 -0.06648 1.542 1.54
1 301928-2218 DUT0_MEM_ADD<3> 301928-2218 DUT0 AC6 301928-2218 129 D01 386 9 399 9 987 -0.05852 1.54 1.538
1 301928-2218 DUT0_MEM_ADD<4> 301928-2218 DUT0 AB8 301928-2218 118 D15 388 5 399 9 988 6 -0.03863 1.352 1.348
1 301928-2218 DUT0_MEM_ADD<6> 301928-2218 DUT0 AB9 301928-2218 118 D16 388 8 400 988 8 -0.03675 1.334 1.334
1 301928-2218 DUT0_MEM_ADD<1> 301928-2218 DUT0 V7 301928-2218 119 D08 388 8 399 9 988 9 -0.07075 1.321 1.321
1 301928-2218 DUT0_MEM_ADD<10> 301928-2218 DUT0 AA8 301928-2218 119 D12 389 3 399 9 989 4 -0.05123 1.26 1.261
1 301928-2218 DUT0_MEM_ADD<7> 301928-2218 DUT0 AC5 301928-2218 119 D12 389 6 400 989 6 -0.02783 1.247 1.246
1 301928-2218 DUT0_MEM_ADD<7> 301928-2218 DUT0 AA9 301928-2218 119 D14 389 6 400 989 6 -0.04469 1.242 1.24
1 301928-2218 DUT0_MEM_ADD<0> 301928-2218 DUT0 V8 301928-2218 117 D13 391 7 400 991 7 -0.05333 0.9807 0.9755
1 301928-2218 DUT0_MEM_ADD<8> 301928-2218 DUT0 AB10 301928-2218 117 D15 391 8 400 992 -0.03467 0.9715 0.9667
1 301928-2218 DUT0_MEM_ADD<11> 301928-2218 DUT0 V9 301928-2218 117 D16 391 8 400 991 9 -0.06621 0.9654 0.9607
*****

*****
Pulse Data Per Xnet
*****
XNet      PulseFreq  PulseDutyCycle  PulseCycleCount
-----
1 301928-2218 DUT0_MEM_ADD<9> 100MHz  0.5  1
1 301928-2218 DUT0_MEM_ADD<8> 100MHz  0.5  1
1 301928-2218 DUT0_MEM_ADD<7> 100MHz  0.5  1
1 301928-2218 DUT0_MEM_ADD<6> 100MHz  0.5  1
1 301928-2218 DUT0_MEM_ADD<5> 100MHz  0.5  1
1 301928-2218 DUT0_MEM_ADD<4> 100MHz  0.5  1
1 301928-2218 DUT0_MEM_ADD<3> 100MHz  0.5  1
1 301928-2218 DUT0_MEM_ADD<2> 100MHz  0.5  1
1 301928-2218 DUT0_MEM_ADD<1> 100MHz  0.5  1

```

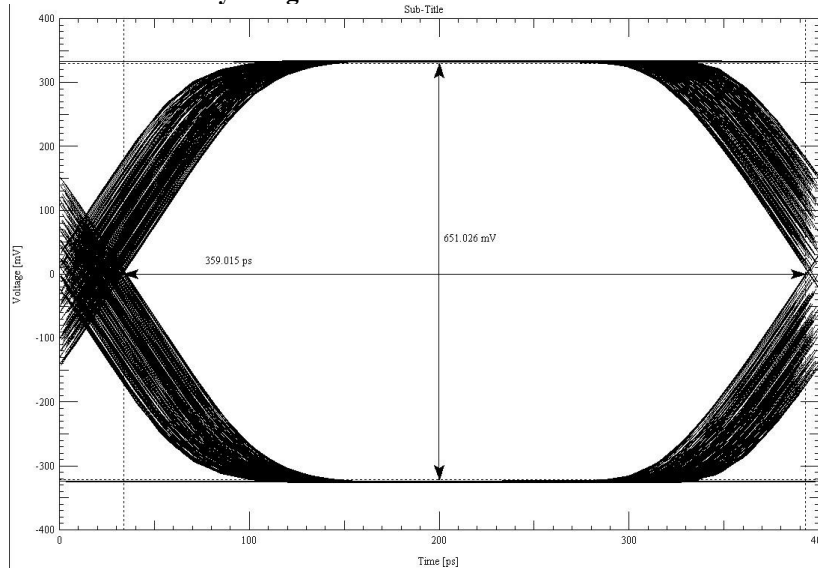
Return & Insertion loss analysis:

Dielectric and Skin effect losses dominate in the high speed designs. Return loss and insertion loss analysis are done for high speed PCIe signals, to verify the required eye opening, according to the spec. The following picture shows the eye opening of around 9.5 inch PCIe signal at the receiver, generated with 1000 bits, 10% UI transmitted jitter. The eye opening is around 651 mV which is well above the spec of 175 mV, at the receiver. The maximum length of the PCIe signal has been constrained as 10 inches during Pre layout analysis and the design has been routed with approximately 9.5 inches trace length. The extracted topology in the SigXplorer is shown below:





Eye diagram with 1000 bits simulation



Mixed mode S parameter was taken for the PCIe differential pairs to determine the performance of the differential pair under the following conditions.

1 Differential signal in-Differential signal out (**Insertion loss**)

2. Indicates pure differential mode conversion.

3 Differential signal in -Common signal out

4. Indicates the generation of EMI from the differential pairs.

5 Common signal in -Common signal out

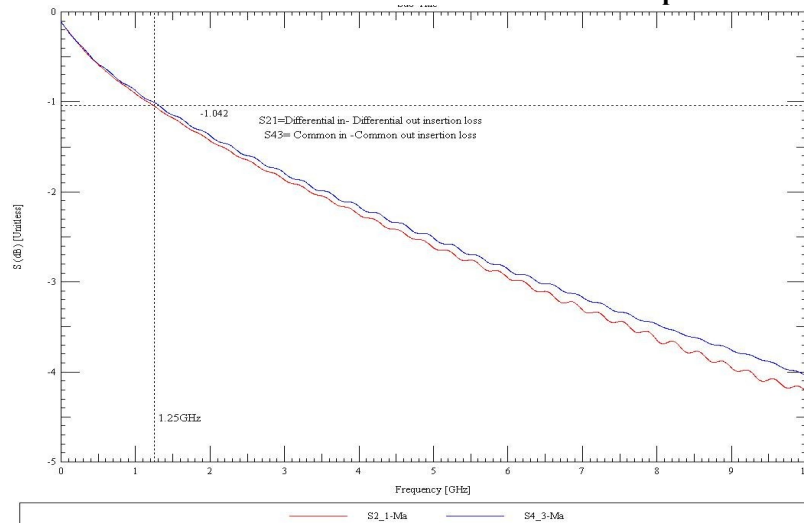
6. Indicates the performance of the device under common mode.

7 Common signal in- Differential signal out

8. Indicates the susceptibility to EMI of the diff pairs.

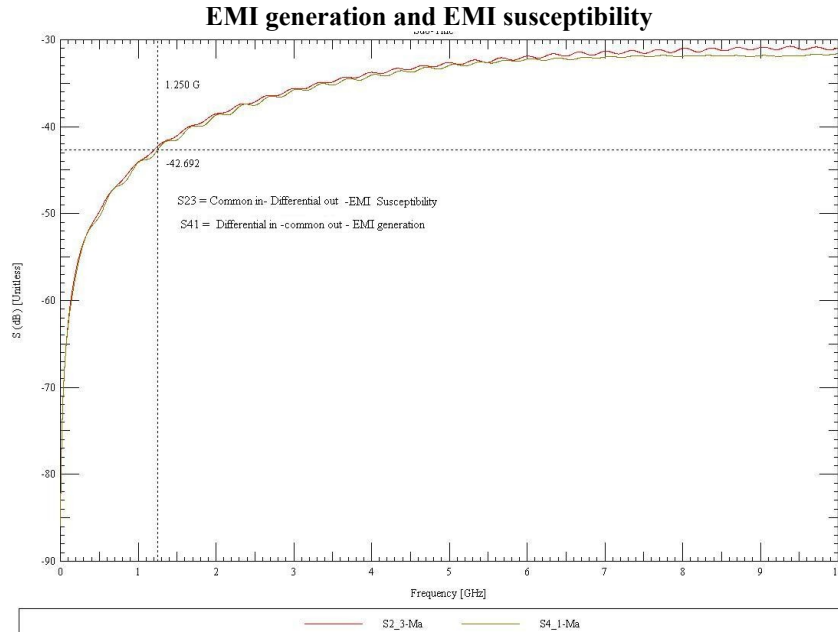
As the following picture shows the differential pair of length 9.5 inches has insertion loss of around -1dB, for common and differential signal inputs.

Insertion Loss for Common and Differential Input



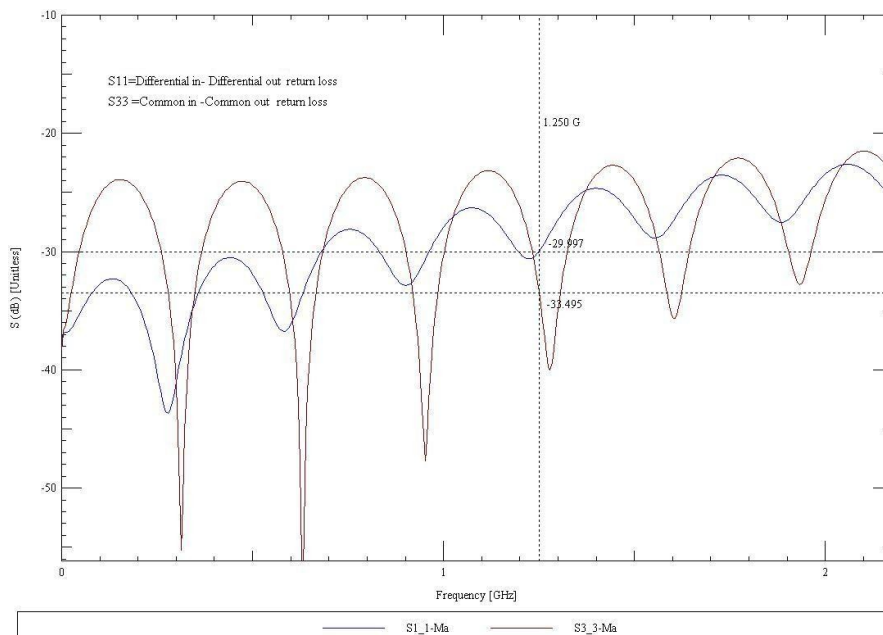


Also the following picture shows that, with the value of around -42dB, the PCIe differential pair has good EMI susceptibility and generates less interference



The return loss of the 9.5 inch differential pair at 1.25GHz is about -29.9 dB for differential input and -33.495 dB for common mode signal and the picture is shown below.

Differential and Common signal Return loss

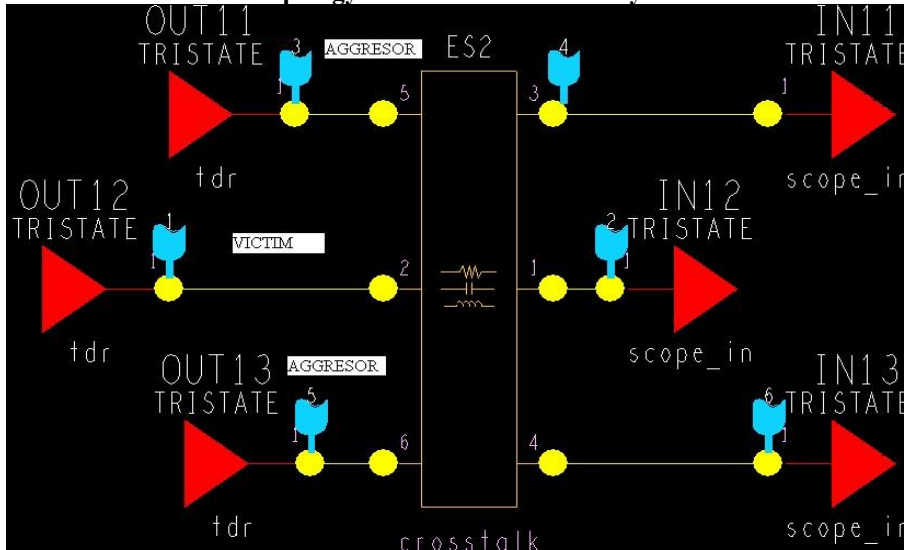




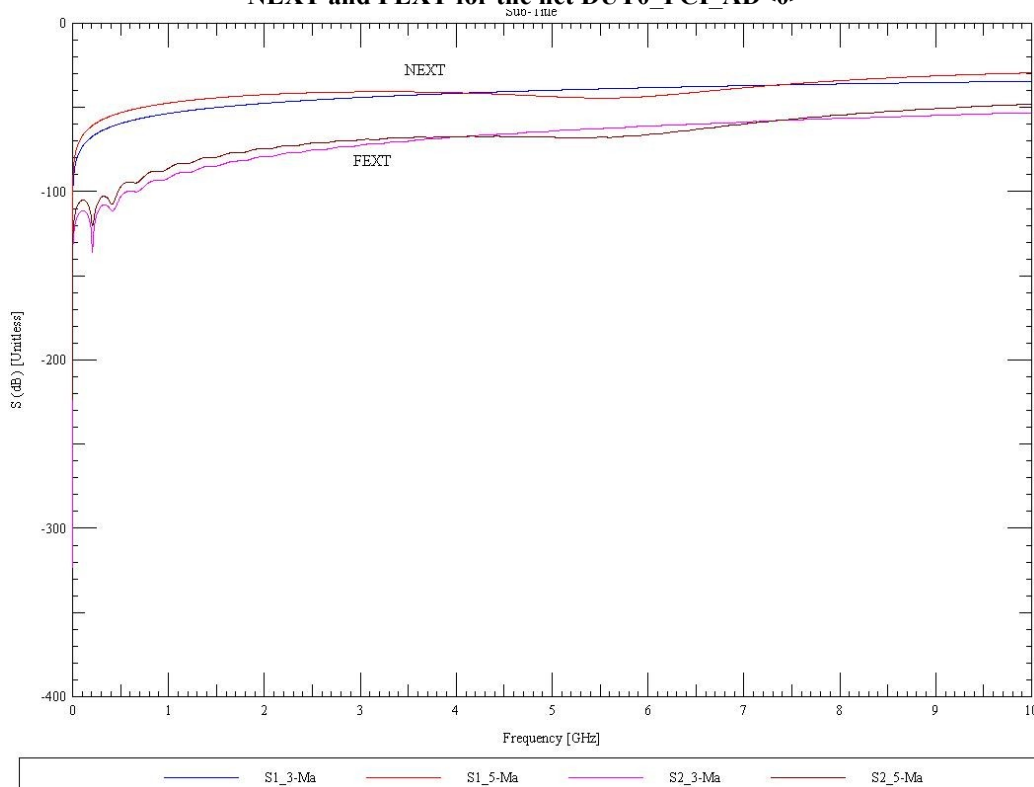
Crosstalk analysis:

The single ended traces in the design has been routed with 6.5 mils trace width and minimum spacing of 2x. Following figures shows the NEXT and FEXT of the net DUT0_PCI_AD<0>. Coupled Espice model is extracted from the Layout board to SigXplorer and S parameter has been generated. The NEXT and FEXT value is about -100dB, indicating that the routing for this net is immune to crosstalk. The topology used is shown below.

Topology used for Crosstalk analysis



NEXT and FEXT for the net DUT0_PCI_AD<0>





DC/AC resistance and Delay analysis:

In order to decrease the losses in the trace, constant impedance and low DC resistance has to be maintained in the routing. The Parasitic report has been taken to verify the AC resistance (Characteristic Impedance) and DC resistance of the nets. Parasitic report and propagation delay of the nets are shown below.

Parasitic report

```
#####
# Allegro PCB SI 630 (SPECCTRAquest)
# 15.51 p006 (v15-5.1-43E) [11/15/2005]
#
# (c) Copyright 1998-2004 Cadence Design Systems, Inc.
#
# Report: Standard Parasitics Report
#
#####

*****
XNet Parasitics
*****
XNet
-----
1 301928-2218 DUT1_MEM_DATA<9> 49.89 61.78 2.804e-011 7.061e-008 1.257
1 301928-2218 DUT1_MEM_DATA<8> 49.89 61.78 2.783e-011 7.016e-008 1.25
1 301928-2218 DUT1_MEM_DATA<7> 49.89 61.78 2.476e-011 6.177e-008 1.091
1 301928-2218 DUT1_MEM_DATA<6> 49.89 61.78 2.71e-011 6.785e-008 1.202
1 301928-2218 DUT1_MEM_DATA<5> 49.89 49.89 1.79e-011 4.456e-008 0.7852
1 301928-2218 DUT1_MEM_DATA<4> 49.89 61.78 2.668e-011 6.729e-008 1.2
1 301928-2218 DUT1_MEM_DATA<3> 49.89 61.78 2.553e-011 6.423e-008 1.143
1 301928-2218 DUT1_MEM_DATA<31> 49.89 61.78 2.86e-011 7.243e-008 1.296
1 301928-2218 DUT1_MEM_DATA<30> 49.89 49.89 2.052e-011 5.108e-008 0.9002
1 301928-2218 DUT1_MEM_DATA<2> 49.89 49.89 1.826e-011 4.545e-008 0.8009
1 301928-2218 DUT1_MEM_DATA<29> 49.89 61.78 2.466e-011 6.149e-008 1.086
```

Propagation Delay Report

```
#
# (c) Copyright 1998-2004 Cadence Design Systems, Inc.
#
# Report: Standard Delay Report
#
#####

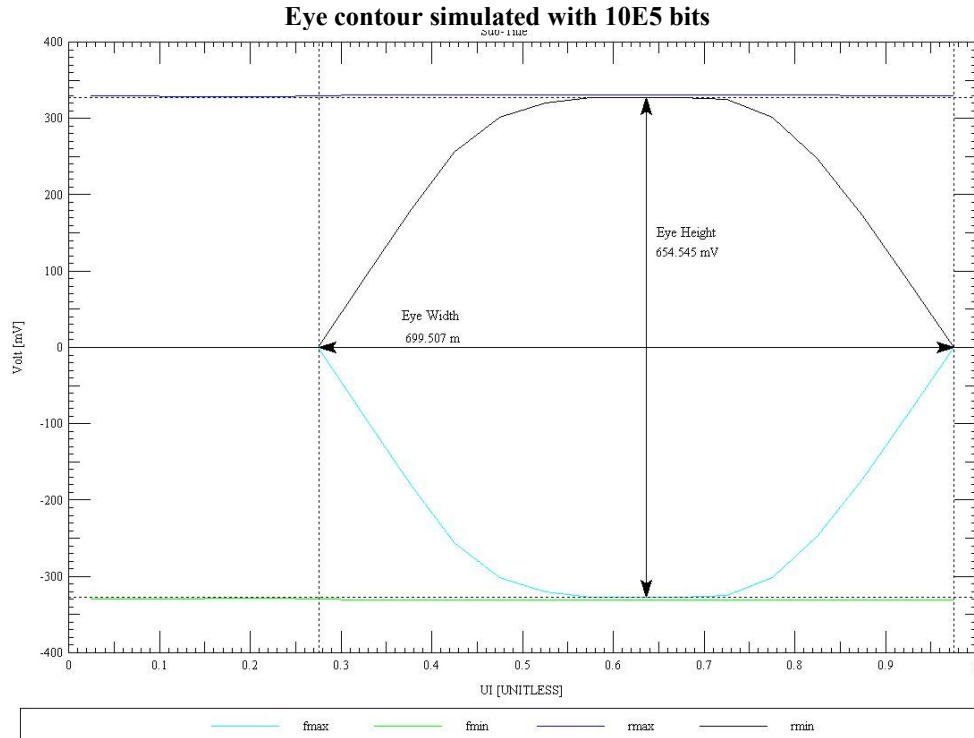
*****
Delays (ns) (Typ FTSMode)
*****
XNet
-----
1 301928-2218 DUT1_MEM_DATA<31> 301928-2218 DUT1 W6 301928-2218 116 D05 1.438 1.475 1.473 1.515
1 301928-2218 DUT1_MEM_DATA<9> 301928-2218 DUT1 T12 301928-2218 108 D13 1.406 1.451 1.45 1.476
1 301928-2218 DUT1_MEM_DATA<8> 301928-2218 DUT1 V12 301928-2218 111 D01 1.396 1.468 1.406 1.504
1 301928-2218 DUT1_MEM_DATA<1> 301928-2218 DUT1 W13 301928-2218 108 D12 1.367 1.418 1.416 1.448
1 301928-2218 DUT1_MEM_DATA<6> 301928-2218 DUT1 W12 301928-2218 108 D11 1.356 1.405 1.398 1.439
1 301928-2218 DUT1_MEM_DATA<14> 301928-2218 DUT1 V13 301928-2218 111 D02 1.355 1.403 1.396 1.438
1 301928-2218 DUT1_MEM_DATA<4> 301928-2218 DUT1 T13 301928-2218 108 D06 1.339 1.38 1.374 1.42
1 301928-2218 DUT1_MEM_DATA<0> 301928-2218 DUT1 V14 301928-2218 108 D05 1.325 1.366 1.361 1.396
1 301928-2218 DUT1_MEM_DATA<15> 301928-2218 DUT1 W14 301928-2218 108 D04 1.296 1.344 1.342 1.368
1 301928-2218 DUT1_MEM_DATA<10> 301928-2218 DUT1 AA13 301928-2218 108 D03 1.293 1.34 1.339 1.364
1 301928-2218 DUT1_MEM_DATA<3> 301928-2218 DUT1 AA14 301928-2218 107 D16 1.28 1.328 1.328 1.353
1 301928-2218 DUT1_MEM_DATA<11> 301928-2218 DUT1 AB14 301928-2218 107 D15 1.265 1.314 1.314 1.343
1 301928-2218 DUT1_MEM_DATA<23> 301928-2218 DUT1 V5 301928-2218 107 D05 1.247 1.285 1.288 1.326
1 301928-2218 DUT1_MEM_DATA<7> 301928-2218 DUT1 AB13 301928-2218 107 D14 1.237 1.272 1.274 1.308
1 301928-2218 DUT1_MEM_DATA<29> 301928-2218 DUT1 AB4 301928-2218 107 D09 1.231 1.267 1.269 1.3
1 301928-2218 DUT1_MEM_DATA<28> 301928-2218 DUT1 AB3 301928-2218 107 D08 1.211 1.254 1.254 1.28
1 301928-2218 DUT1_MEM_DATA<24> 301928-2218 DUT1 V6 301928-2218 106 D11 1.204 1.25 1.249 1.274
```

Propagation Delay Matching (skew):

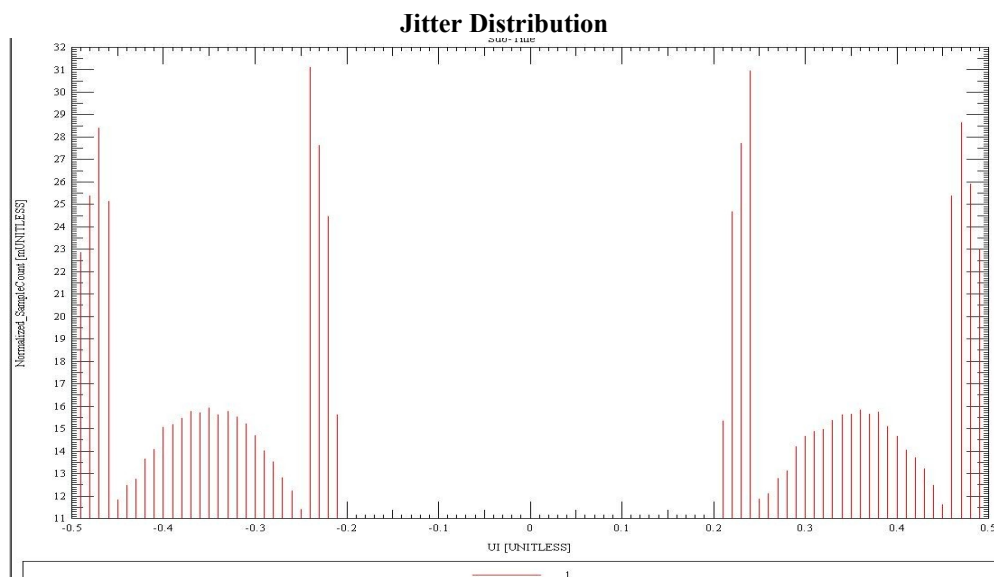
Skew between the differential line traces generates common mode current in the return path [3]. In order to control EMI generation, common mode current must be minimized. For PCIe differential signals, skew of less than 30 mils is allowed. The following diagram shows the eye contour of 9.5 inch PCIe signal, routed with skew of around 10 mils.



The channel analysis report of PCIe signals simulated with 10E5 bits with 8b10b encoding and 25% UI transmitter jitter is shown below. Eye width of .699 UI and height of 654mV indicates good signal reception at the receiver pins [1].



The jitter distribution and the channel analysis report at the receiver are shown below.





```
Channel Simulation report
Channel Analysis Report
File Close Help
***Channel Analysis Report*****

Channel Inputs:
  Bit period           = 4e-010
  No of drivers        = 1
  No of taps           = 1
  Tap optimization     = No
  Stimulus configuration = poly23
  Channel coding       = 8
  Char Directory       = D:\SI_project\Load_board_case_study\sigxp.run/ca:

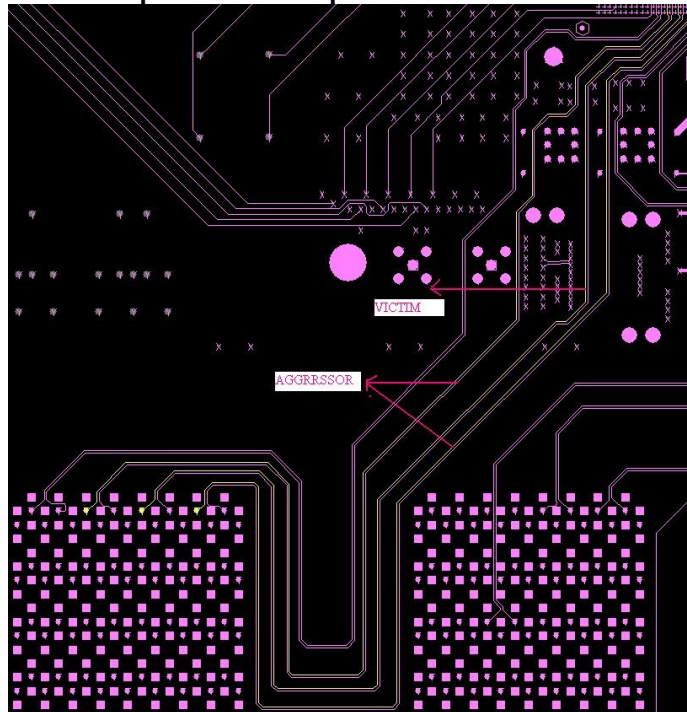
Simulation Controls:
  No of bits simulated = 1000000
  Measurement Delay    = 1e-007

Eye Measurements:
  Eye height           = 654 mV
  UI at max height    = 0.575 UI
  Eye jitter           = 0.3 UI
```

Analysis of three coupled Differential pairs:

The design has been analysed for three coupled differential pairs, to verify if the spacing between them is sufficient to avoid crosstalk. A snapshot the differential pairs in the layout is shown below.

Coupled differential pairs routed in the board

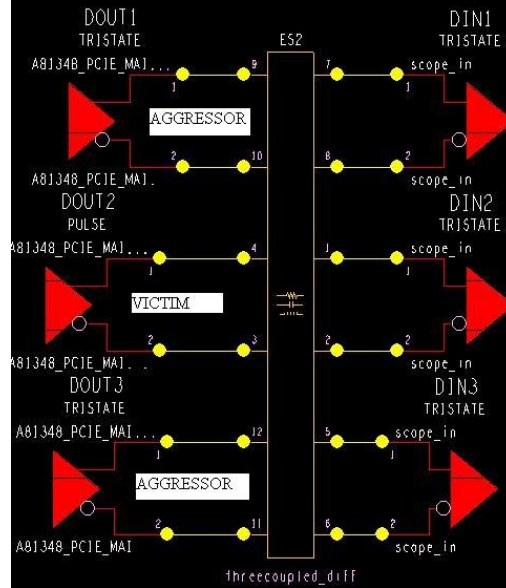


Espsice model of the three coupled differential pairs are extracted from the board and taken to the SigXplorer, for channel analysis. The differential pairs are routed in the board with 6 mil trace width and 12 mils inter-pair spacing. The minimum intra-pair spacing maintained is 30 mils. The drivers are modeled using Intel



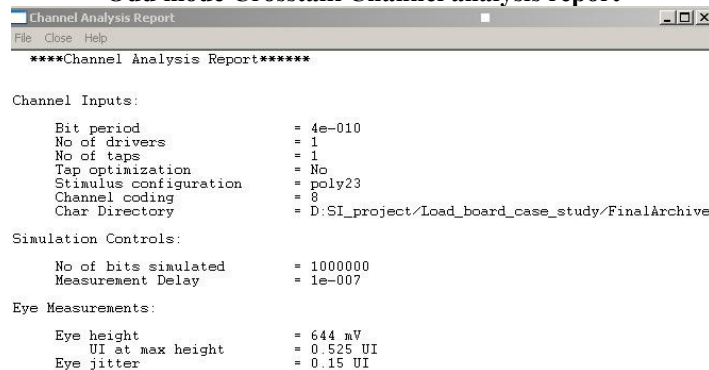
81348 IO processor's PCIe model, so that the results will be comparable to the real world scenario. The Espice topology is shown below.

Espice Topology of Coupled Differential pairs



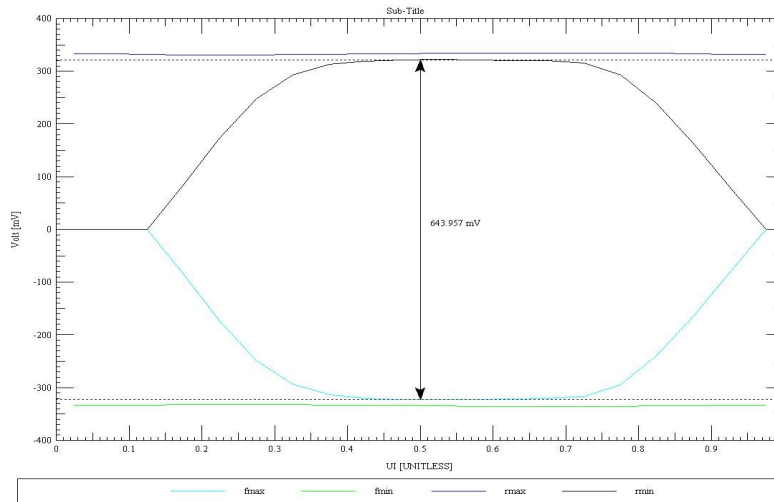
Channel analysis has been done at 2.5Gbps, with 10%UI transmitter jitter and 1E6 bits. The length of the routed interconnect is about 9500 mils. The channel analysis report for odd mode crosstalk is given below.

Odd mode Crosstalk Channel analysis report





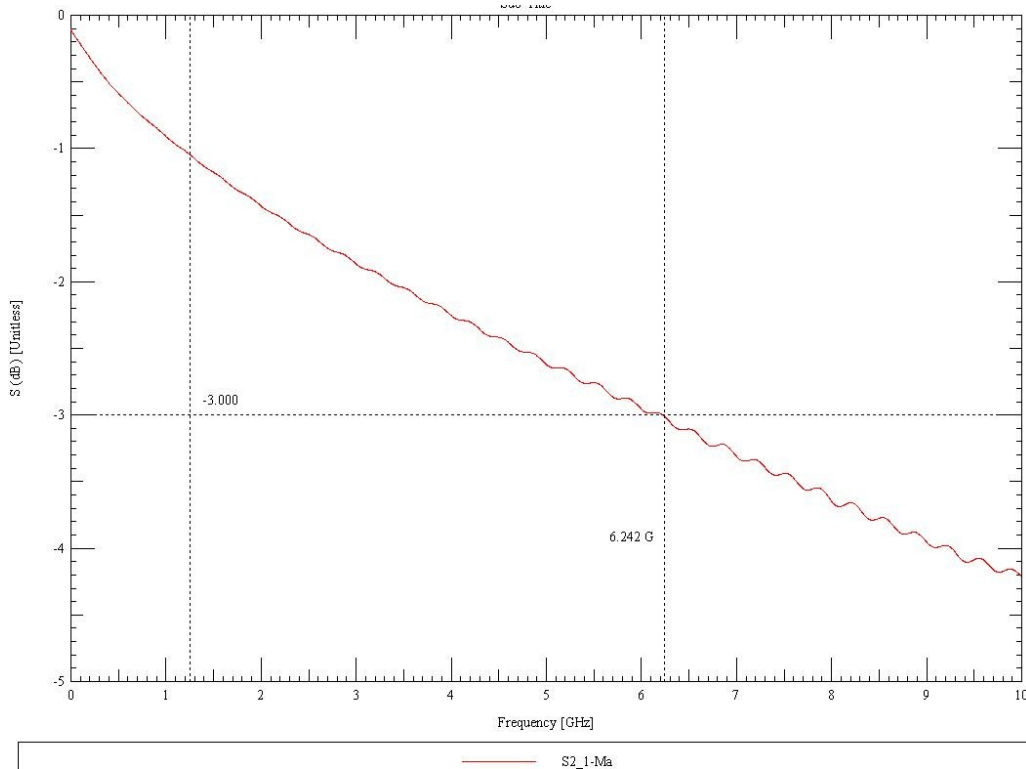
Eye Contour for odd mode Crosstalk Channel analysis



Interconnect Bandwidth Verification:

Dielectric losses dominate in the Gigabit designs. Bandwidth of the interconnect is increased by Various techniques, such as using equalization technique in case of low cost FR4 material, using low loss tangent materials like Rogers. The -3dB bandwidth of the 9.5 inch PCIe interconnect is about 6 GHz. So this interconnect can transmit the PCIe signals faithfully, from DUT to POGO pins [2].

Bandwidth of PCIe Interconnect





Conclusion:

Detailed analysis has been done for the load board designed for the Verigy 93K tester. Post layout analysis has been done to check if the DUT board performs well, so that the DUT can be characterised accurately in the tester. High speed signal like PCIe, which has got data rate of 2.5Gbps, has been analysed in an elaborate manner with the mixed mode S parameter. Analysis showed that the DUT board will perform well with good Signal integrity for both high speed and low speed signals.

REFERENCES

- ← Board Design Guidelines for PCI Express™ Architecture, Cliff Lee, Intel Corporation.
- ← Influence of Dielectric Materials on ATE Test Fixtures for High-Speed Digital Applications, Proceedings of the Sixth International Kharkov Symposium on Physics and Engineering of Microwave, Millimeter and Submillimeter Waves (MSMW'07).
- ← Signal integrity issues and printed circuit board, Douglas Brooks, Prentice Hall PTR.