



Pre-Layout SI analysis of Load Board for Verigy 93000 Tester

Introduction:

The scope of this work is to determine the pre-layout constraint of the load board for Verigy 93000 Tester. The load board analysis is done for the PCIe interface signals, at 2.5 Gbps and defines the following constraints for the board.

- 1 Stackup definition
- 250 Ohm Single Ended Impedance constraints
- 3100 Ohm Differential Impedance constraints
- 4 Constraints for 1 dB Insertion loss in the load board
- 5 Maximum length allowed, for the DC resistance of 4 Ohms.
- 6 Cross talk Study
- 7 Eye opening study for the PCIe signals.

Tools Used:

- Allegro Sigxplorer.
- Allegro PCB SI

Stackup definition:

Hybrid stackup is defined in this board that uses NELCO 4000-13 and ROGERS 4350. PCIe signals are constrained to route with ROGERS 4350 dielectrics. The stackup was designed for 6 digital signal layers and 3 Analog signal layers. The total thickness was 160 mils and the layer span is 28 layers.

50 Ohm Impedance:

The trace widths to maintain 50 ohm impedance for single ended signals on the different layers of the stackup is shown below.

Subclass Name	Type	Material	Thickness (MIL)	Conductivity (mho/cm)	Dielectric Constant	Loss Tangent	Negative Artwork	Shield	Width (MIL)	Impedance (ohm)
1	SURFACE	AIR								
2	TOP	CONDUCTOR	COPPER	1.4	595900	3.800000	0.008	<input type="checkbox"/>		
3		DIELECTRIC	NELCO_4000_13	5	0	3.800000	0.008		9.000	52.488
4	DGND1	PLANE	COPPER	0.7	595900	3.800000	0.008	<input type="checkbox"/>	<input checked="" type="checkbox"/>	
5		DIELECTRIC	ROGERS_4350	8	0	3.500000	0.0031			
6	DSIG1	CONDUCTOR	COPPER	0.7	595900	3.500000	0.0031	<input type="checkbox"/>		8.000
7		DIELECTRIC	ROGERS_4350	8	0	3.500000	0.0031			
8	DGND2	PLANE	COPPER	0.7	595900	3.800000	0.008	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
9		DIELECTRIC	NELCO_4000_13	7	0	3.800000	0.008			
10	DSIG2	CONDUCTOR	COPPER	0.7	595900	3.800000	0.008	<input type="checkbox"/>		6.500
11		DIELECTRIC	NELCO_4000_13	7	0	3.800000	0.008			
12	DGND3	PLANE	COPPER	0.7	595900	3.800000	0.008	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
13		DIELECTRIC	NELCO_4000_13	7	0	3.800000	0.008			
14	DSIG3	CONDUCTOR	COPPER	0.7	595900	3.800000	0.008	<input type="checkbox"/>		6.500
15		DIELECTRIC	NELCO_4000_13	7	0	3.800000	0.008			
16	DGND4	PLANE	COPPER	0.7	595900	3.800000	0.008	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	



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100 Ohm definition:

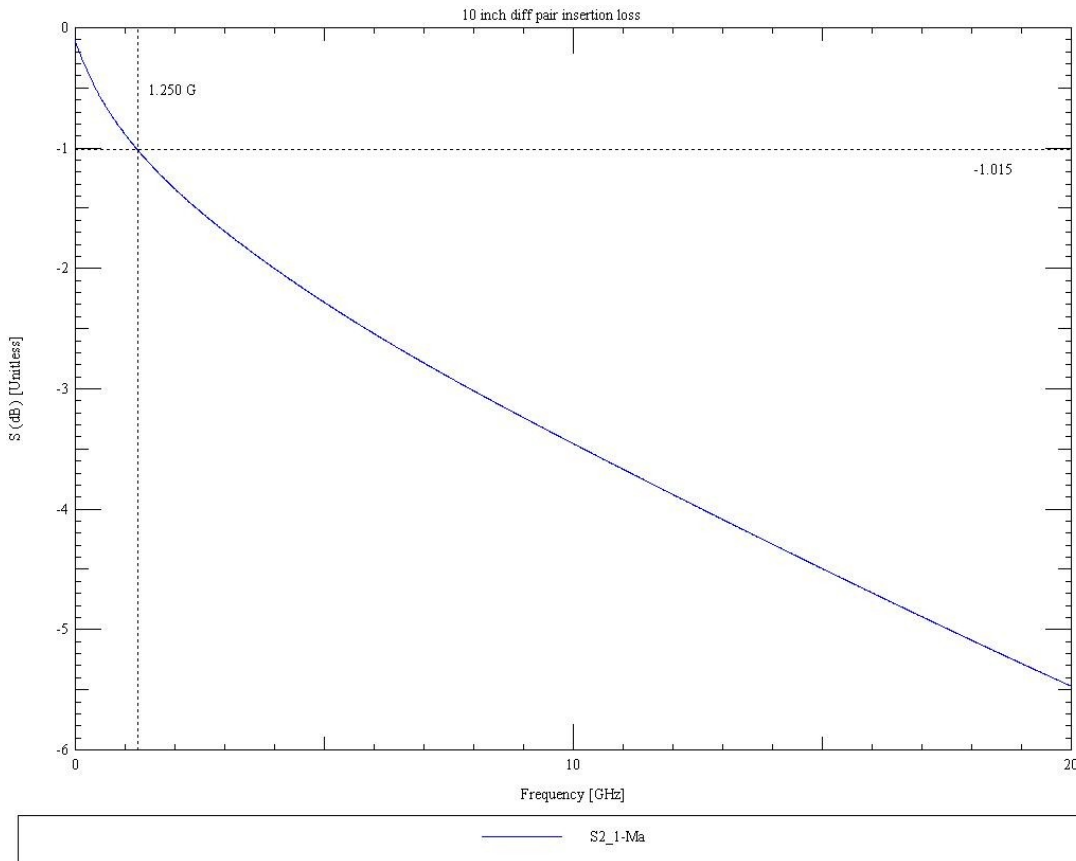
The PCIe signals are constrained with 7.5 mils trace width and it is optimized for its bandwidth of 1.25 GHz. The trace width and spacing for the differential signals on the layers are shown below.

Subclass Name	Type	Thickness (MIL)	Dielectric Constant	Loss Tangent	Shield	Width (MIL)	Impedance (ohm)	Coupling Type	Spacing (MIL)	DiffZ0 (ohm)
1	SURFACE									
2	TOP	CONDUCTOR	1.4	3.800000	0.008	9.000		NONE		
3		DIELECTRIC	5	3.800000	0.008					
4	DGND1	PLANE	0.7	3.800000	0.008					
5		DIELECTRIC	8	3.500000	0.0031					
6	DSIG1	CONDUCTOR	0.7	3.500000	0.0031	7.500		EDGE	15.000	101.83
7		DIELECTRIC	8	3.500000	0.0031					
8	DGND2	PLANE	0.7	3.800000	0.008					
9		DIELECTRIC	7	3.800000	0.008					
10	DSIG2	CONDUCTOR	0.7	3.800000	0.008	6.000		EDGE	12.000	100.5
11		DIELECTRIC	7	3.800000	0.008					
12	DGND3	PLANE	0.7	3.800000	0.008					
13		DIELECTRIC	7	3.800000	0.008					
14	DSIG3	CONDUCTOR	0.7	3.800000	0.008	6.000		EDGE	12.000	100.5
15		DIELECTRIC	7	3.800000	0.008					
16	DGND4	PLANE	0.7	3.800000	0.008					

Constraints for 1 dB Insertion loss in the load board:

The Insertion loss allowed in the dut board at 1.25GHz is 1 dB for PCIe signals and the length of the trace that corresponds to 1 dB loss is determined as 10 inches. The insertion loss is shown below.

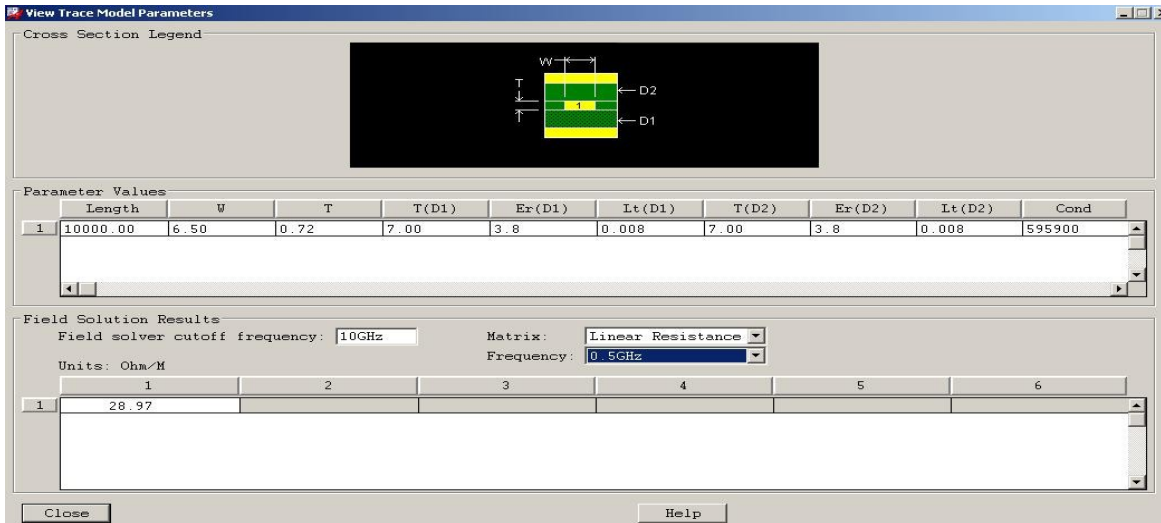
10 inch Diff pair Insertion loss





DC resistance calculation:

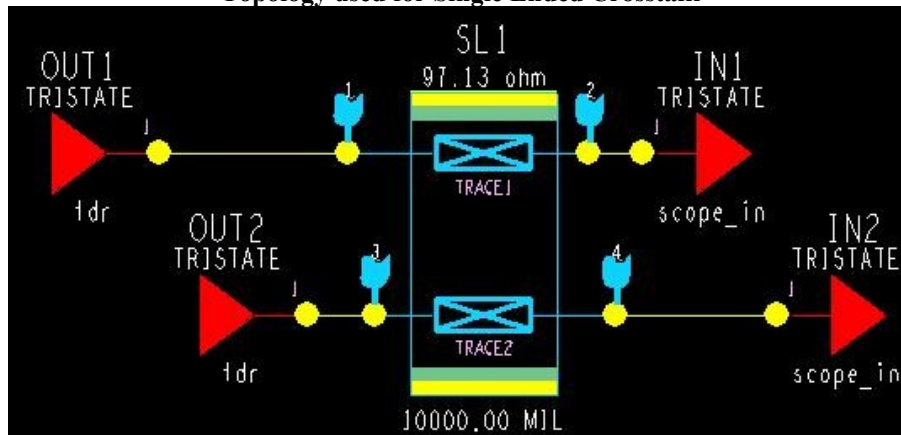
The max DC resistance allowed in the single ended trace was 4 ohm and the maximum length of the 50 Ohm (characteristic Impedance) single ended trace that meets this specification, at 500 MHz, was calculated as 5.4 inches.



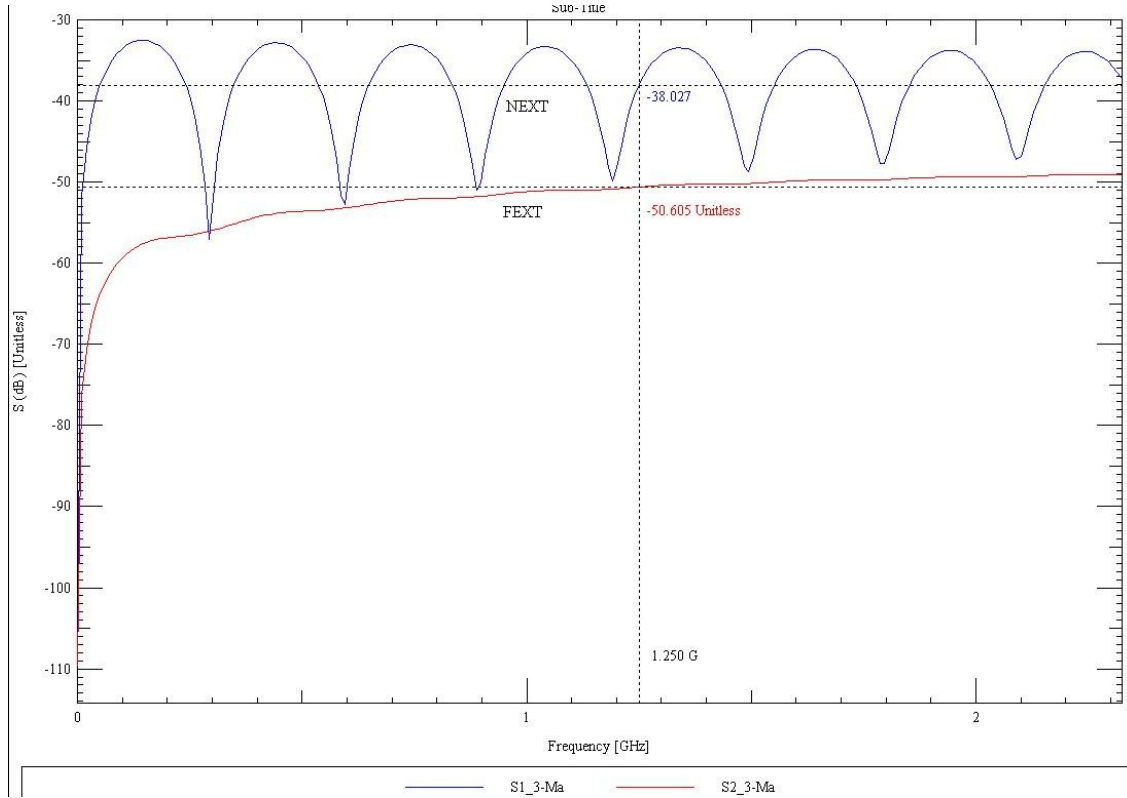
Crosstalk Study:

For minimum spacing of 2X (13 mils) and length of 10 inch, the NEXT and FEXT are obtained as shown as below. The drivers have been modeled using TDR model and the receiver as 50 ohm inputs. NEXT is -38.192 dB and FEXT is -50.371 dB.

Topology used for Single Ended Crosstalk



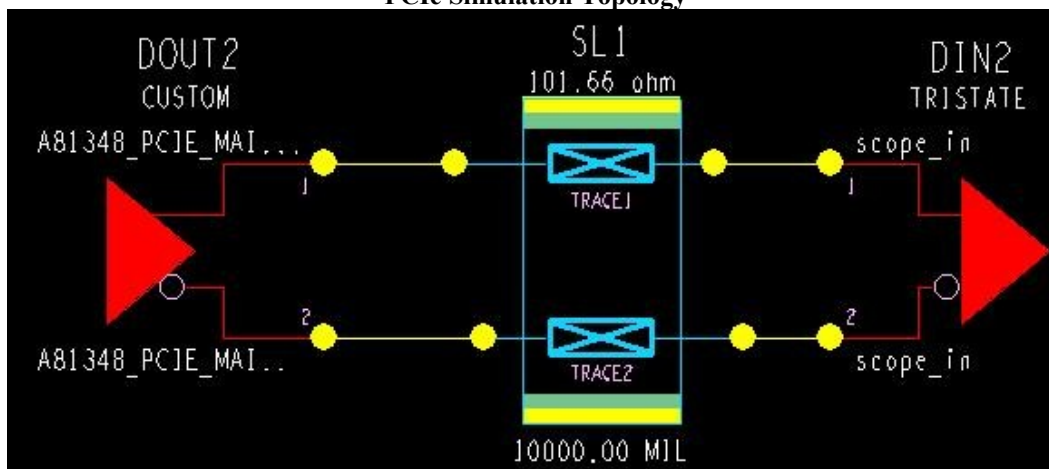
NEXT and FEXT for Single Ended Signal



Eye opening study for the PCIe signals:

Eye opening is studied for the PCIe signal, to verify if the specified trace length meets the PCIe spec. The transmitter is modeled, using the PCIe buffer model of the 81348 Intel I/O processor, so that the simulation will give close results when compared to the actual buffer used in the DUT. Simulation was done for 1E6 bits with 5% UI transmitter jitter. The simulation topology, receiver's channel simulation report and the eye contour are shown below.

PCIe Simulation Topology



Channel Analysis Report



****Channel Analysis Report****

Channel Inputs:

Bit period = 4e-010
No of drivers = 1
No of taps = 1
Tap optimization = No
Stimulus configuration = poly23
Channel coding = 8
Char Directory =

D:\SI_project\Load_board_case_study\sigxp.run\case0\channel.run\sim2\char\

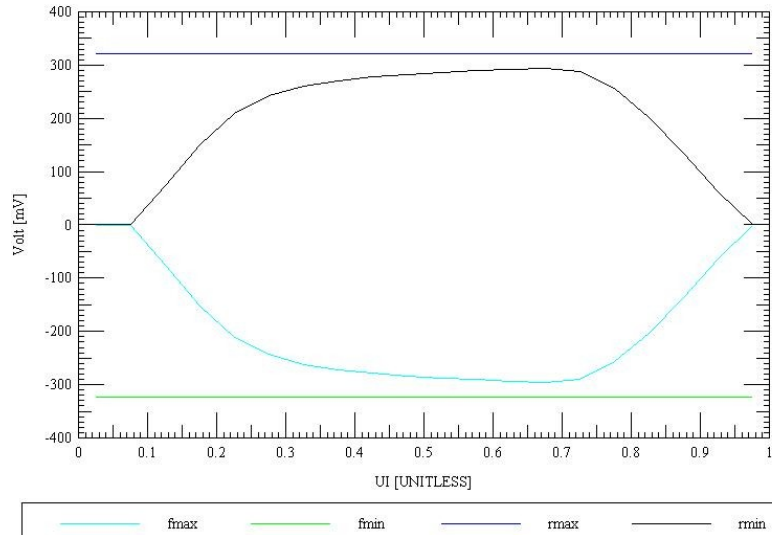
Simulation Controls:

No of bits simulated = 1000000
Measurement Delay = 1e-007

Eye Measurements:

Eye height = 588 mV
UI at max height = 0.675 UI
Eye jitter = 0.1 UI

Eye contour for 10 inch diff pair

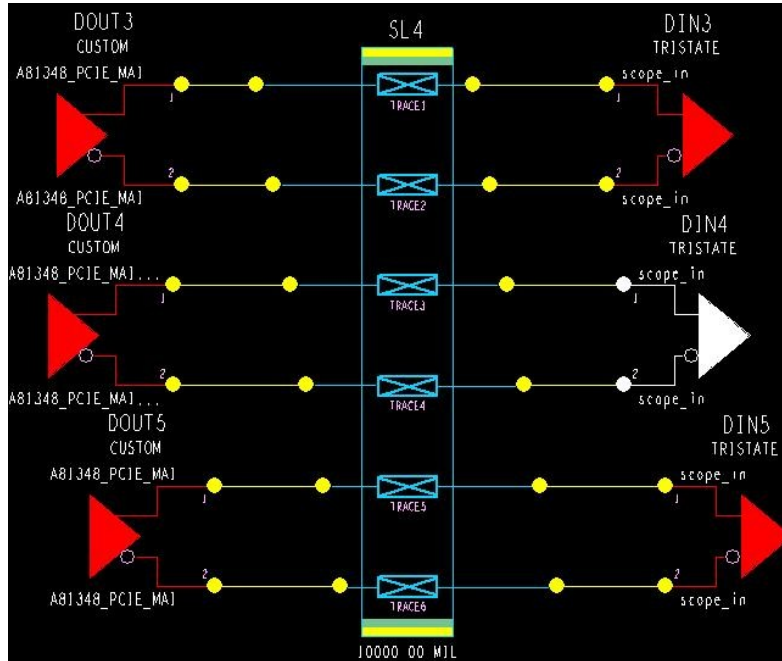


The eye-height is 588mV and the eye duration is around 0.9 UI, which is well above the spec of 175mV and 0.4UI respectively[1].

The variation of the eyeheight with crosstalk is studied and is shown below with 1x and 2x intra-pair spacing. When 1X(7.5mils) is maintained between the diffpairs the eyeheight reduces and the corresponding topology along with channel simulation report is shown below. Simulation is done with 1E6 bits and 10%UI transmitter jitter.



Topology used for Crosstalk Simulation



1X spacing channel simulation report

*****Channel Analysis Report*****

Channel Inputs:

Bit period = 4e-010
No of drivers = 3
No of taps = 1
Tap optimization = No
Stimulus configuration = poly23
Channel coding = 8
Char Directory =

D:\SI_project\Load_board_case_study\Crosstalk\sigxp.run\case0\channel1.run\sim1\char\

Simulation Controls:

No of bits simulated = 1000000
Measurement Delay = 1e-007

Eye Measurements:

Eye height = 575 mV
UI at max height = 0.675 UI
Eye jitter = 0.15 UI



2X spacing channel simulation report

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****Channel Analysis Report*****
Wed Jun 04 15:10:00 2008

Channel Inputs:

  Bit period           = 4e-010
  No of drivers        = 3
  No of taps           = 1
  Tap optimization     = NO
  Stimulus configuration = poly23
  Channel coding        = 8
  Char Directory       =
D:\SI_project\Load_board_case_study\Crosstalk\sigxp.run\case0\channel.
run\2x_spacing\char/

Simulation Controls:

  No of bits simulated = 1000000
  Measurement Delay    = 1e-007

Eye Measurements:

  Eye height           = 583 mV
  UI at max height     = 0.675 UI
  Eye jitter           = 0.15 UI
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Conclusion:

The load board for the verigy 93K tester was pre simulated and the impedance, spacing constraints, for the single ended and differential signals are determined as shown above. Using the channel analysis, the PCIe signals are constrained so that the PCIe specification is met. Based on the above analysis following constraints have been given for the design.

←6.5 mils trace width for the single ended signals, to achieve 50 Ohms characteristic impedance and 7.5 mils trace width, with 15 mils inter-pair spacing, to achieve differential impedance of 100 Ohms.

←For 1 dB insertion loss in the board, the maximum length of the PCIe differential signal is constrained as 10 inches.

←For DC resistance of 4 Ohms in the single ended signals, the maximum trace length are calculated

←Based on S parameter based NEXT and FEXT analysis, 2X spacing has been constrained between single ended traces to have minimum crosstalk.

←For PCIe signals, variation of eye-height due to crosstalk is studied for 1X and 2x intra-pair spacing. 1X spacing has insertion loss of -2.86 dB and 2x spacing has insertion loss of -2.74 dB. So 2X spacing has been constrained for the PCIe pairs.[1]

Reference:

1. Board Design Guidelines for PCI Express™ Architecture, Cliff Lee, Intel Corporation.