



Overview

This case study describes the PCB layout design and SI analysis of the interface between DDR-II memory controller in a DSP processor with the two On board DDR-II 533 Mbps memory chips. Each chip has 2 bytes of data group. Processor also has video port signals. The board is designed for the application of video processing for automobile industry.

Objective

The objective is to design the board for the specific application with good signal integrity by performing pre-layout and post-layout SI analysis of the design having DDR-II 533 Mbps signals.

Tools Used

Expedition PCB 2005 – PCB Layout Design
Hyperlynx – SI Analysis

Stack-up

Number of layers : 14
Single ended impedance : 50 ohm
Differential impedance : 100ohm



50 ohm impedance definition

| Basic Dielectric Metal Z0 Planning Custom View | | | | | | | | | | |
|--|-------------------------------------|-------------|-----------------|------------|------------|-----------|----------------|--------|-----------------|--------|
| | Visible | Color | Pour Draw Style | Layer Name | Type | Usage | Thickness mils | Er | Test Width mils | Z0 ohm |
| 1 | <input checked="" type="checkbox"/> | Red | Hatched | 1 | Metal | Signal | 1.35 | <Auto> | 6 | 51.9 |
| 2 | | | | | Dielectric | Substrate | 3.77 | 4.3 | | |
| 3 | <input checked="" type="checkbox"/> | Yellow | Hatched | 2 | Metal | Plane | 0.675 | <Auto> | 6 | 69.3 |
| 4 | | | | | Dielectric | Substrate | 4.00 | 4.3 | | |
| 5 | <input checked="" type="checkbox"/> | Magenta | Hatched | 3 | Metal | Signal | 0.675 | <Auto> | 4 | 50.6 |
| 6 | | | | | Dielectric | Substrate | 4.05 | 4.3 | | |
| 7 | <input checked="" type="checkbox"/> | Blue | Hatched | 4 | Metal | Signal | 0.675 | <Auto> | 4 | 50.6 |
| 8 | | | | | Dielectric | Substrate | 4.00 | 4.3 | | |
| 9 | <input checked="" type="checkbox"/> | Orange | Hatched | 5 | Metal | Plane | 0.675 | <Auto> | 6 | 41.8 |
| 10 | | | | | Dielectric | Substrate | 3.66 | 4.3 | | |
| 11 | <input checked="" type="checkbox"/> | Cyan | Hatched | 6 | Metal | Plane | 0.675 | <Auto> | 6 | 41.5 |
| 12 | | | | | Dielectric | Substrate | 3.5 | 4.3 | | |
| 13 | <input checked="" type="checkbox"/> | Dark Red | Hatched | 7 | Metal | Signal | 0.675 | <Auto> | 3.5 | 50.6 |
| 14 | | | | | Dielectric | Substrate | 4.05 | 4.3 | | |
| 15 | <input checked="" type="checkbox"/> | Green | Hatched | 8 | Metal | Signal | 0.675 | <Auto> | 3.5 | 50.6 |
| 16 | | | | | Dielectric | Substrate | 3.5 | 4.3 | | |
| 17 | <input checked="" type="checkbox"/> | Purple | Hatched | 9 | Metal | Plane | 0.675 | <Auto> | 6 | 41.5 |
| 18 | | | | | Dielectric | Substrate | 3.66 | 4.3 | | |
| 19 | <input checked="" type="checkbox"/> | Teal | Hatched | 10 | Metal | Plane | 0.675 | <Auto> | 6 | 41.8 |
| 20 | | | | | Dielectric | Substrate | 4.00 | 4.3 | | |
| 21 | <input checked="" type="checkbox"/> | Dark Blue | Hatched | 11 | Metal | Signal | 0.675 | <Auto> | 4 | 50.6 |
| 22 | | | | | Dielectric | Substrate | 4.05 | 4.3 | | |
| 23 | <input checked="" type="checkbox"/> | Light Green | Hatched | 12 | Metal | Signal | 0.675 | <Auto> | 4 | 50.6 |
| 24 | | | | | Dielectric | Substrate | 4.00 | 4.3 | | |
| 25 | <input checked="" type="checkbox"/> | Red | Hatched | 13 | Metal | Plane | 0.675 | <Auto> | 6 | 69.3 |
| 26 | | | | | Dielectric | Substrate | 3.77 | 4.3 | | |
| 27 | <input checked="" type="checkbox"/> | Yellow | Hatched | 14 | Metal | Signal | 1.35 | <Auto> | 6 | 51.9 |

100 ohm impedance definition

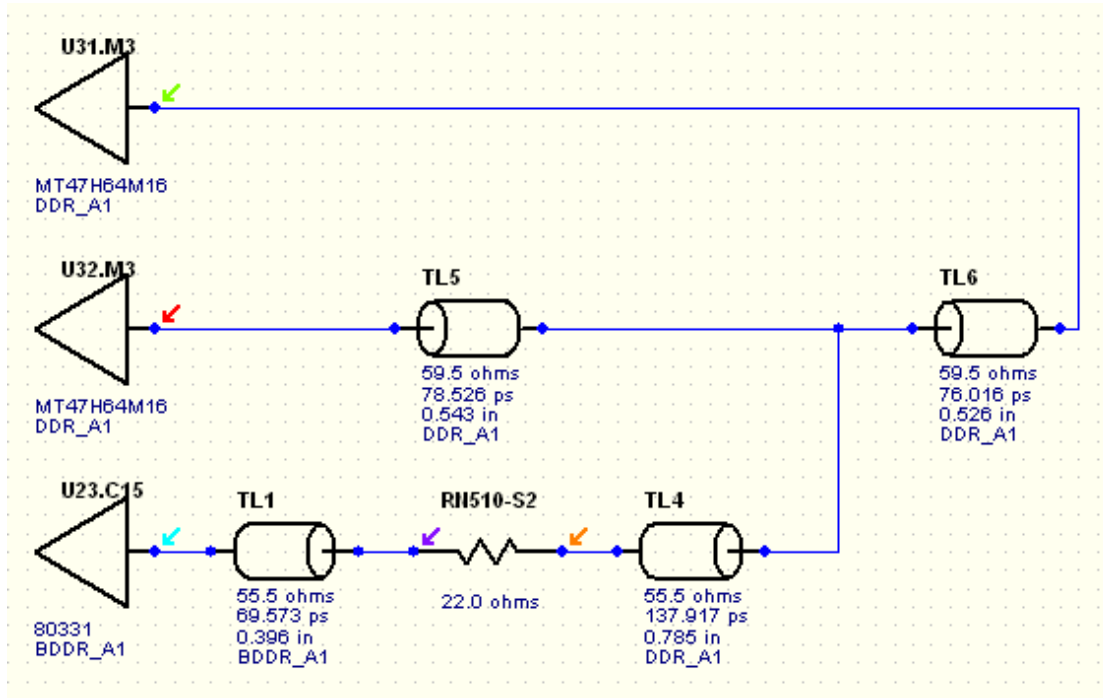
| Basic Dielectric Metal Z0 Planning Custom View | | | | | | | | |
|--|------------|-----------|----------------|--------|-------------|------------|----------|----------|
| | Layer Name | Usage | Thickness mils | Er | Diff Z0 ohm | Width mils | Gap mils | Z0 Curve |
| 1 | 1 | Signal | 1.35 | <Auto> | 100 | 4 | 3.813 | |
| 2 | | Substrate | 3.77 | 4.3 | | | | |
| 3 | 2 | Plane | 0.675 | <Auto> | 75 | 6 | 2.381 | |
| 4 | | Substrate | 4 | 4.3 | | | | |
| 5 | 3 | Signal | 0.675 | <Auto> | 100 | 3.5 | 7.715 | |
| 6 | | Substrate | 4.05 | 4.3 | | | | |
| 7 | 4 | Signal | 0.675 | <Auto> | 100 | 3.5 | 7.715 | |
| 8 | | Substrate | 4 | 4.3 | | | | |
| 9 | 5 | Plane | 0.675 | <Auto> | 75 | 6 | 5.687 | |
| 10 | | Substrate | 3.66 | 4.3 | | | | |
| 11 | 6 | Plane | 0.675 | <Auto> | 75 | 6 | 5.77 | |
| 12 | | Substrate | 3.5 | 4.3 | | | | |
| 13 | 7 | Signal | 0.675 | <Auto> | 100 | 3.2 | 8.216 | |
| 14 | | Substrate | 4.05 | 4.3 | | | | |
| 15 | 8 | Signal | 0.675 | <Auto> | 100 | 3.2 | 8.216 | |
| 16 | | Substrate | 3.5 | 4.3 | | | | |
| 17 | 9 | Plane | 0.675 | <Auto> | 75 | 6 | 5.77 | |
| 18 | | Substrate | 3.66 | 4.3 | | | | |
| 19 | 10 | Plane | 0.675 | <Auto> | 75 | 6 | 5.687 | |
| 20 | | Substrate | 4 | 4.3 | | | | |
| 21 | 11 | Signal | 0.675 | <Auto> | 100 | 3.5 | 7.715 | |
| 22 | | Substrate | 4.05 | 4.3 | | | | |
| 23 | 12 | Signal | 0.675 | <Auto> | 100 | 3.5 | 7.715 | |
| 24 | | Substrate | 4 | 4.3 | | | | |
| 25 | 13 | Plane | 0.675 | <Auto> | 75 | 6 | 2.381 | |
| 26 | | Substrate | 3.77 | 4.3 | | | | |
| 27 | 14 | Signal | 1.35 | <Auto> | 100 | 4 | 3.813 | |



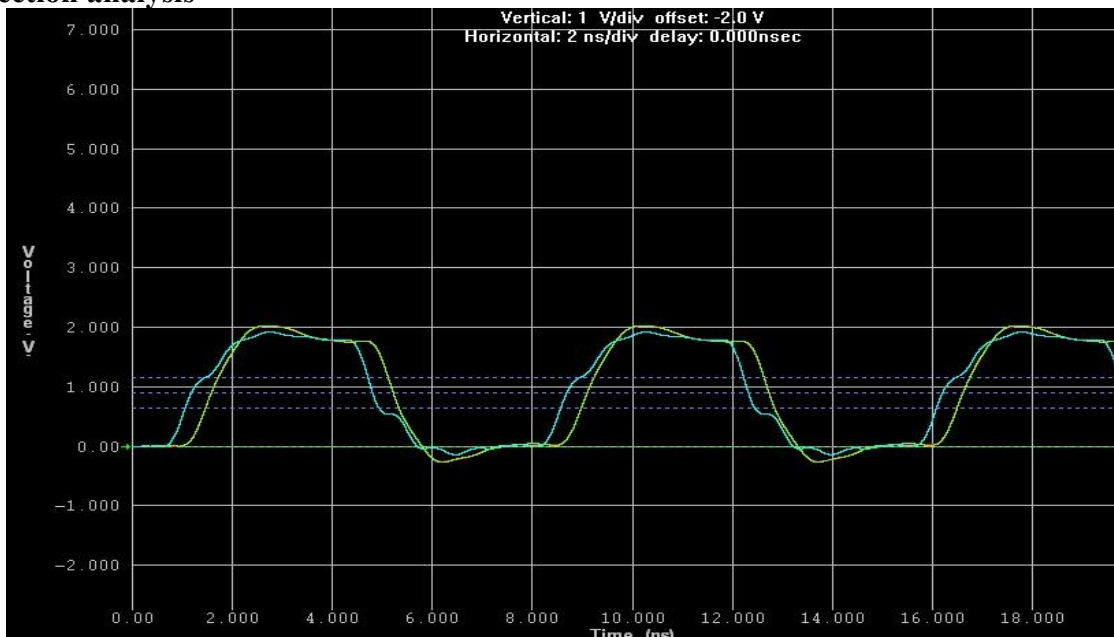
Pre-layout Analysis

Topology optimization

DDR-II address net topology



Reflection analysis





| | |
|--------------|---------------|
| Max. Peak(V) | Min. Peak(mV) |
| 2.03 | -267.3 |

Overshoot and Undershoot values are within the limits (-0.3 to 2.1V)

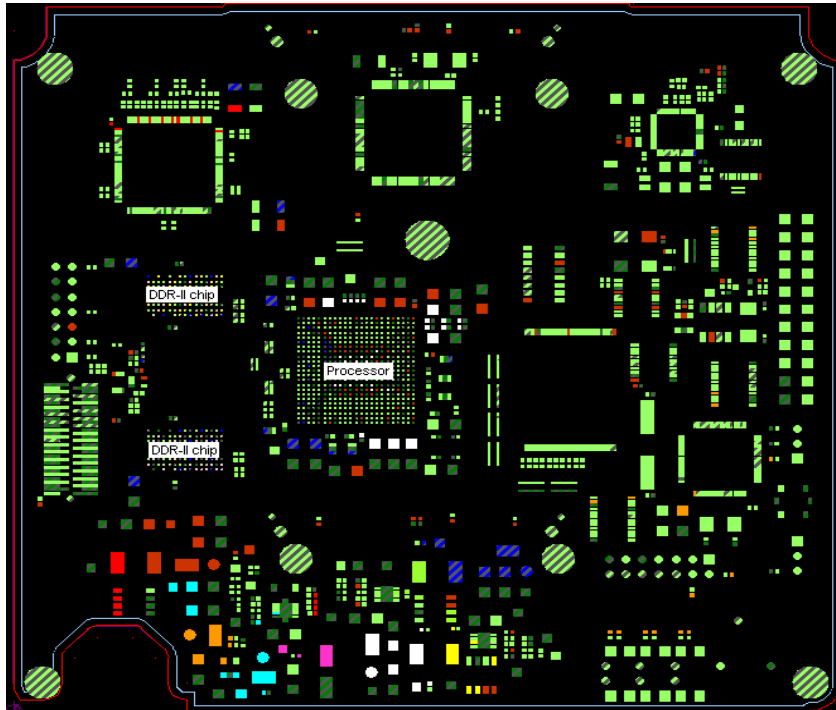
Timing Budget

| DDR-II DATA Write Budget | | | | |
|---|---|--------------|--------------|--------------|
| ELEMENT | SKEW COMPONENT | SETUP | HOLD | UNITS |
| Transmitter | Total Skew at Transmitter | 325 | 325 | ps |
| Clock | Data/Strobe PLL jitter | 25 | 25 | ps |
| DRAM device | tDH/tDS | 100 | 225 | ps |
| | Total Device | 350 | 350 | ps |
| Interconnect | XTK (cross talk) - DQ | 35 | 35 | ps |
| | XTK (cross talk) - DQS | 20 | 20 | ps |
| | ISI - DQ | 30 | 30 | ps |
| | ISI - DQS | 5 | 5 | ps |
| | Input Capacitance Matching | 25 | 25 | ps |
| | REFF Mismatch | 10 | 10 | ps |
| | Input Eye Reduction (VREF) | 25 | 25 | ps |
| | Path Matching(Board) | 10 | 10 | ps |
| Total Interconnect | Interconnect Skew | 160 | 160 | ps |
| Total Budget | 1875/2 at 533 MHz | 937.5 | 937.5 | ps |
| Total Budget Consumed by Controller and DRAM | Transmitter + DRAM +interconnect | 840 | 840 | ps |
| Interconnect Budget | Total-(Transmitter + DRAM +interconnect) | 77.5 | 77.5 | ps |

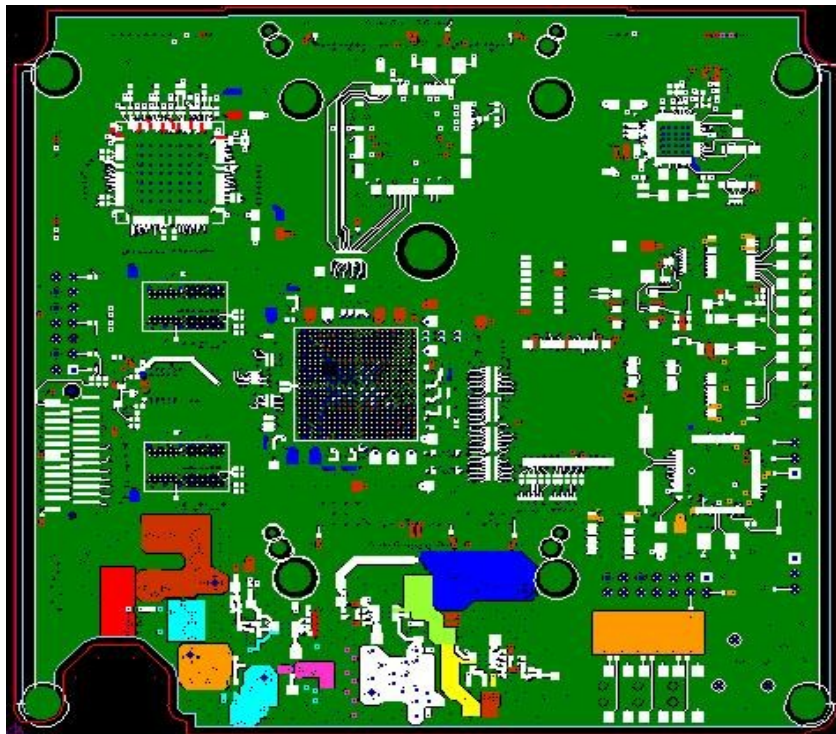
Data and strobe signals of byte is matched within 50 mils



Placement Drawing

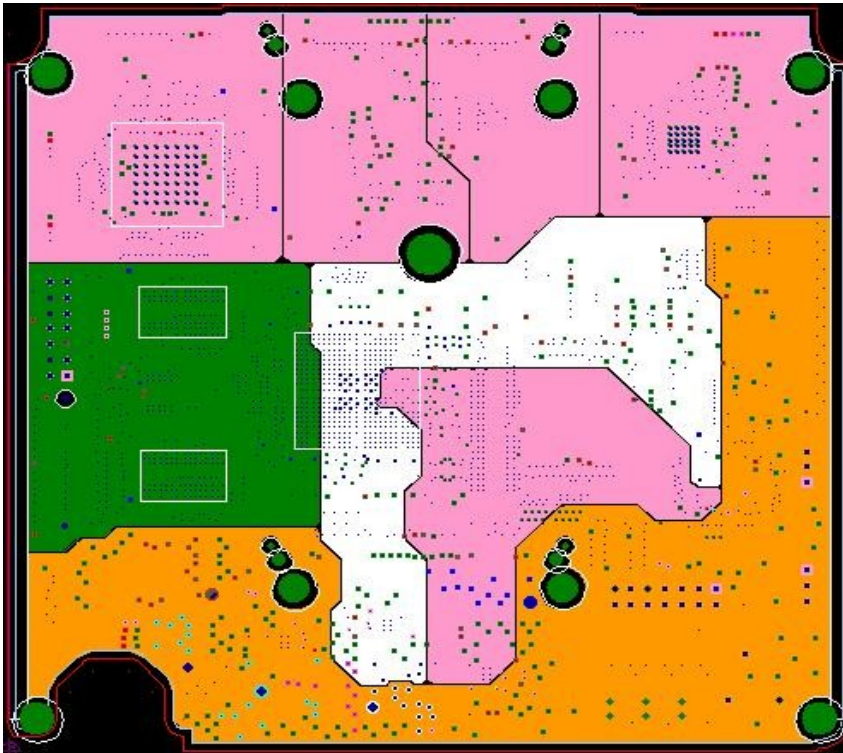


Top Layer

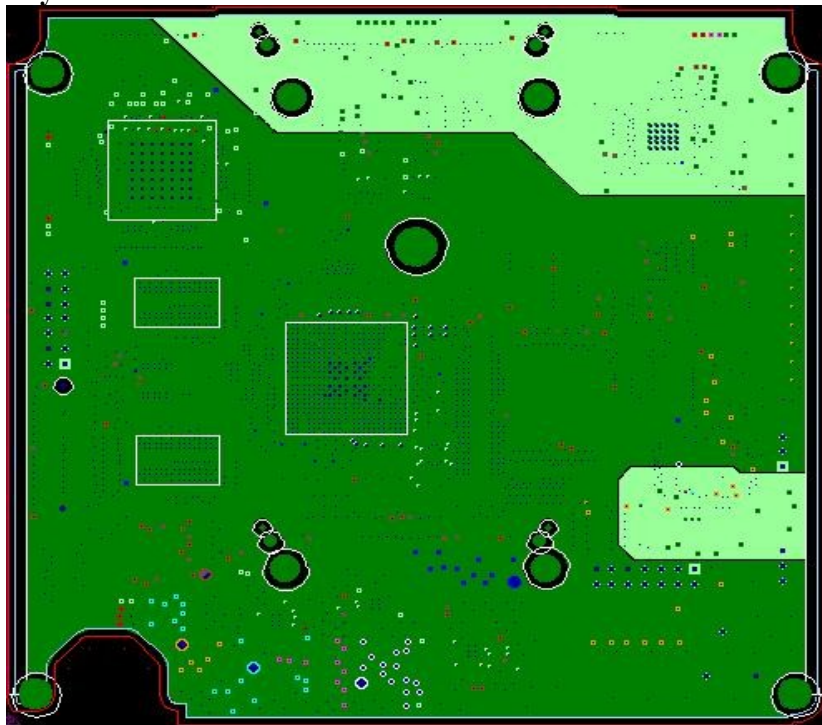




Power Layer



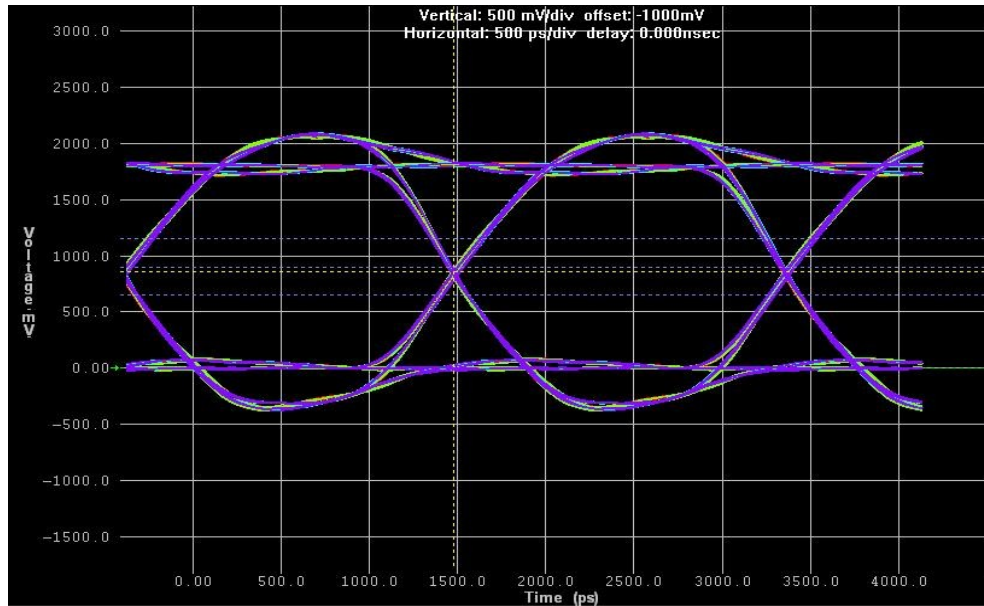
Ground Layer





Post-layout Analysis

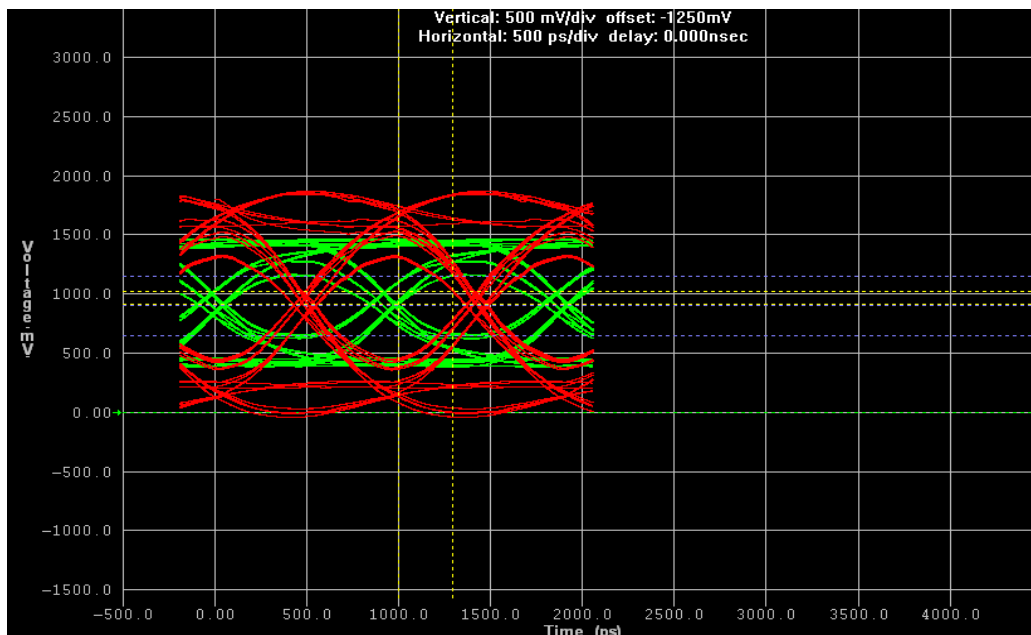
Clock net differential Eye Waveform



Differential cross point (0.858V) is within the limits (0.725 to 1.075V)

Differential Eye height is 1.72V (Required 0.5 to 1.8V)

Timing Analysis – DATA Write



Available input setup & hold time: 107ps & 293ps (Required: 100ps & 225ps)

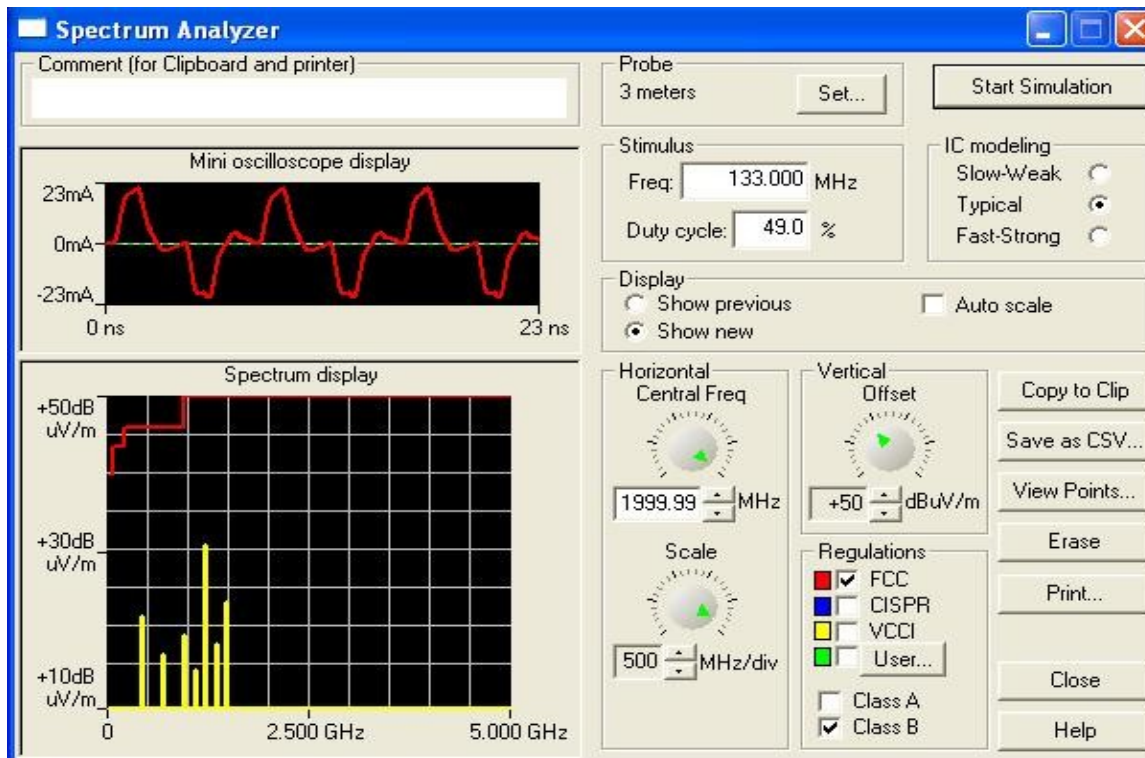


Crosstalk Analysis

| Net(s) | Driver(s) [RefDes.Pin] | Receiver [RefDes.Pin] | Rise/Fall Crosstalk [mV] | Rise/Fall Crosstalk [Pass/Fail] | Total Net Length |
|--------|---------------------------|--------------------------|--------------------------------|---------------------------------------|---------------------|
| DDR_D5 | U32.H9 | U23.D8 | -11 | Pass | 1.591 in |
| DDR_D5 | U23.D8 | U32.H9 | -14 | Pass | 1.591 in |
| DDR_D7 | U32.F9 | U23.E7 | -28 | Pass | 1.590 in |
| DDR_D7 | U23.E7 | U32.F9 | -33 | Pass | 1.590 in |
| DDR_D0 | U23.E9 | U32.G8 | -21 | Pass | 1.591 in |
| DDR_D0 | U32.G8 | U23.E9 | 18 | Pass | 1.591 in |
| DDR_D6 | U32.F1 | U23.C7 | -12 | Pass | 1.584 in |
| DDR_D6 | U23.C7 | U32.F1 | 14 | Pass | 1.584 in |
| DDR_D3 | U32.H3 | U23.C8 | -6 | Pass | 1.578 in |
| DDR_D3 | U23.C8 | U32.H3 | 7 | Pass | 1.578 in |
| DDR_A4 | U23.D14 | U32.N8 | 41 | Pass | 2.289 in |
| DDR_A4 | U23.D14 | U31.N8 | 43 | Pass | 2.289 in |

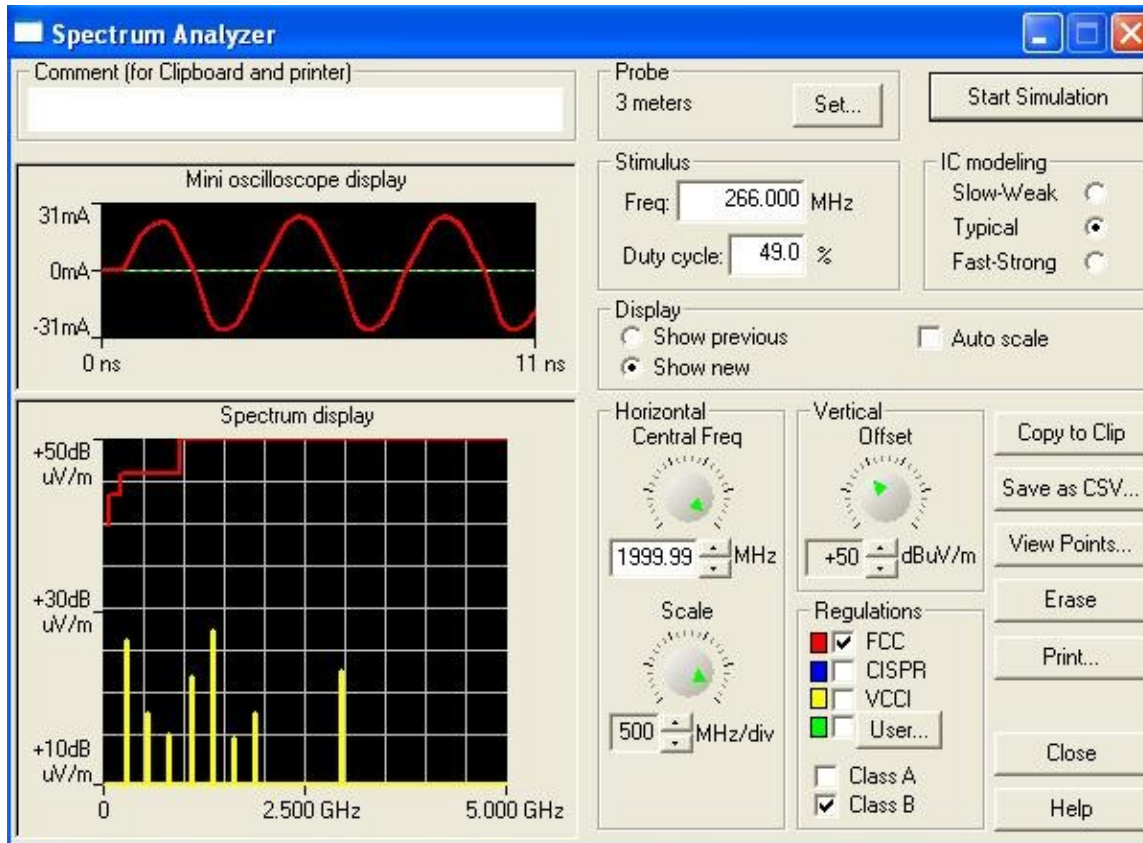
EMI Analysis

DDR-II Address net EMI





DDR-II Data net EMI



Conclusion

The video board PCB layout is designed with specifications developed by performing the pre-layout SI analysis. The design is verified for good signal integrity by post-layout SI analysis and EMI analysis.