



# Post Layout SI Analysis of High Speed PCB

## Introduction:

The sample high speed board is an add-on card to VME bus master. This add-on card has three multicore CPUs, 3x16 512Mb DDR1 RAMs, firewire IC for camera input, camlink/AVI input IC, PCI to VME bus IC etc. Pre-layout and Post-layout SI and timing analysis is done for the two important interfaces viz, CPU to DDR Memory chips and CPU to PCI/VME bus interface.

**Tools used:** Orcad Schematic, Allegro PCB Editor, Allegro PCB SI

## STACKUP:

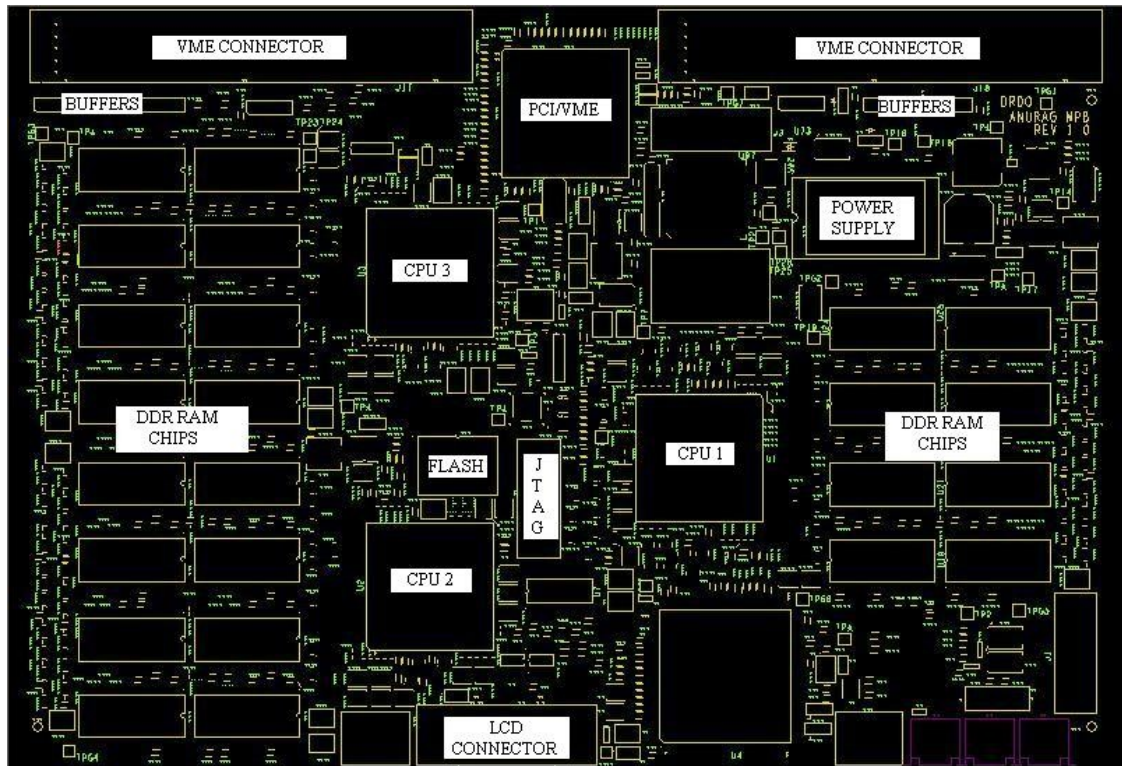
This board is completed with 14 layer stackup. Controlled impedance routing is done for PCI and DDR sections. The stackup has three power layers and three ground layers. The thickness of the board is 96.4 mils, sticking to VME standards. The stackup of the board is shown below

Subclass Name	Type	Material	Thickness (mils)	Conductivity (mho/cm)	Dielectric Constant	Loss Tangent	Negative Artwork	Shield	Width (MIL)	Impedance (ohm)
	SURFACE	AIR								
	DIELECTRIC	CONFORMAL_COAT	1	0	3.00000	0.035				
TOP	CONDUCTOR	COPPER	2.1	595900	3.70000	0.035	<input type="checkbox"/>		3.63	58.782
	DIELECTRIC	FR-4	3.7	0	3.70000	0.035				
PwR1	PLANE	COPPER	0.7	595900	3.70000	0.035	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		
	DIELECTRIC	FR-4	6	0	3.70000	0.035				
SIG1	CONDUCTOR	COPPER	0.7	595900	3.70000	0.035	<input type="checkbox"/>		4.00	60.646
	DIELECTRIC	FR-4	7.2	0	3.70000	0.035				
GND1	PLANE	COPPER	0.7	595900	3.70000	0.035	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		
	DIELECTRIC	FR-4	5	0	3.70000	0.035				
SIG2	CONDUCTOR	COPPER	0.7	595900	3.70000	0.035	<input type="checkbox"/>		4.60	60.036
	DIELECTRIC	FR-4	9	0	3.70000	0.035				
SIG3	CONDUCTOR	COPPER	1.4	595900	3.70000	0.035	<input type="checkbox"/>		3.94	59.954
	DIELECTRIC	FR-4	5	0	3.70000	0.035				
PwR2	PLANE	COPPER	1.4	595900	3.70000	0.035	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		
	DIELECTRIC	FR-4	7.2	0	3.70000	0.035				
GND2	PLANE	COPPER	1.4	595900	3.70000	0.035	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		
	DIELECTRIC	FR-4	5	0	3.70000	0.035				
SIG4	CONDUCTOR	COPPER	1.4	595900	3.70000	0.035	<input type="checkbox"/>		6.00	50.658
	DIELECTRIC	FR-4	9	0	3.70000	0.035				
SIG5	CONDUCTOR	COPPER	0.7	595900	3.70000	0.035	<input type="checkbox"/>		6.00	53.447
	DIELECTRIC	FR-4	5	0	3.70000	0.035				
PwR3	PLANE	COPPER	0.7	595900	3.70000	0.035	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		
	DIELECTRIC	FR-4	7.2	0	3.70000	0.035				
SIG6	CONDUCTOR	COPPER	0.7	595900	3.70000	0.035	<input type="checkbox"/>		6.00	50.702
	DIELECTRIC	FR-4	6	0	3.70000	0.035				
GND3	PLANE	COPPER	0.7	595900	3.70000	0.035	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		
	DIELECTRIC	FR-4	3.7	0	3.70000	0.035				
BOTTOM	CONDUCTOR	COPPER	2.1	595900	3.70000	0.035	<input type="checkbox"/>		4.00	56.856
	DIELECTRIC	CONFORMAL_COAT	1	0	3.00000	0.035				
	SURFACE	AIR								



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The following figure shows the floor planning of the PCB



## DDR section (333 MHz):

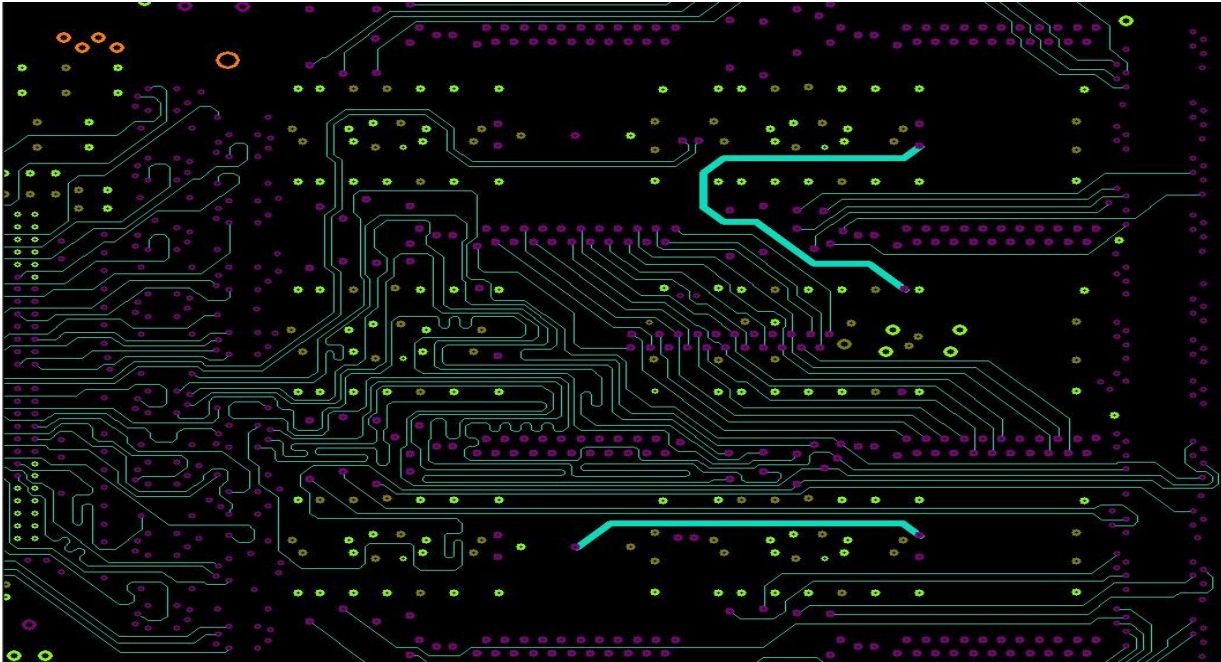
For each Processor, 16 8-bit Embedded DDR1 DRAM chips, each having 512 Mb memory are used to achieve 1GB total capacity. SSTL\_2 standard logic chips with the data rate of 333 MHz are used. DDR section is divided into two Ranks of memory, with each rank having 8 chips. Rank1 and Rank2 chips are placed top and bottom respectively.

DDR signals are routed with 60 ohm impedance. Star topology is used to route DDR signals. Read and Write, Setup and Hold margins, are verified for Address, Data and Control signals. Minimum and maximum lengths of these signals are constrained in the design with respect to the Clock signal. Series and parallel termination are used, for the Address and Data signals, and the values are optimized during prelayout analysis. Reflection and crosstalk analysis is done to see the quality of the routed signals.

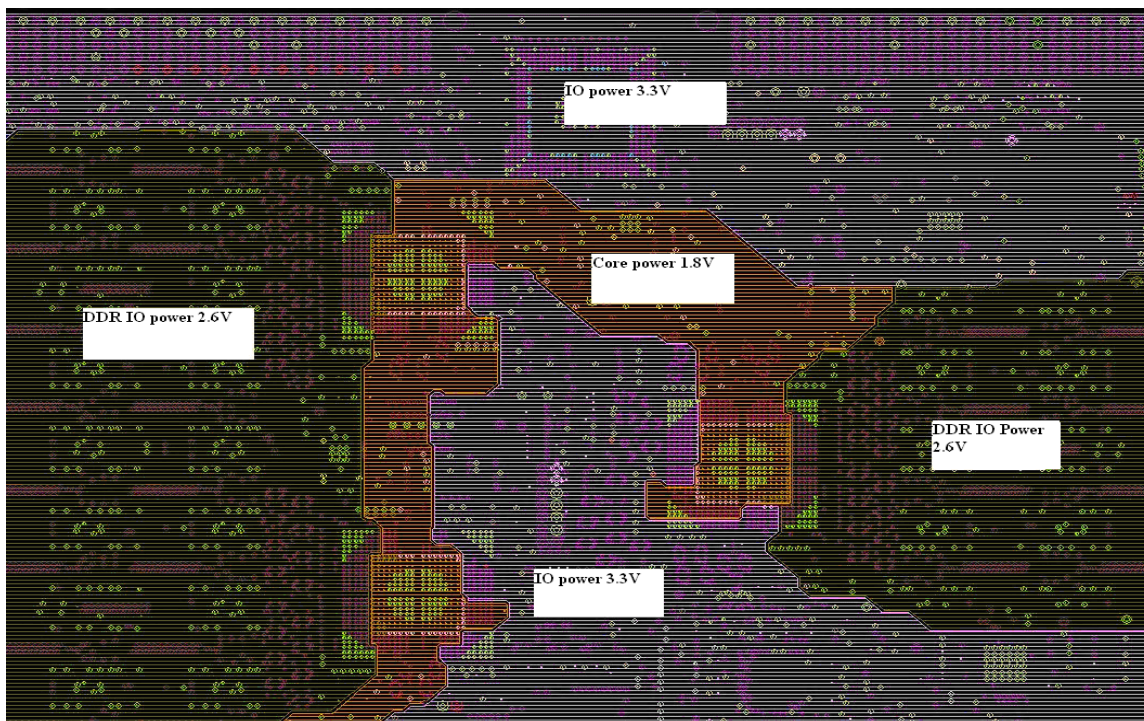


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Below is the sample routing for DDR section



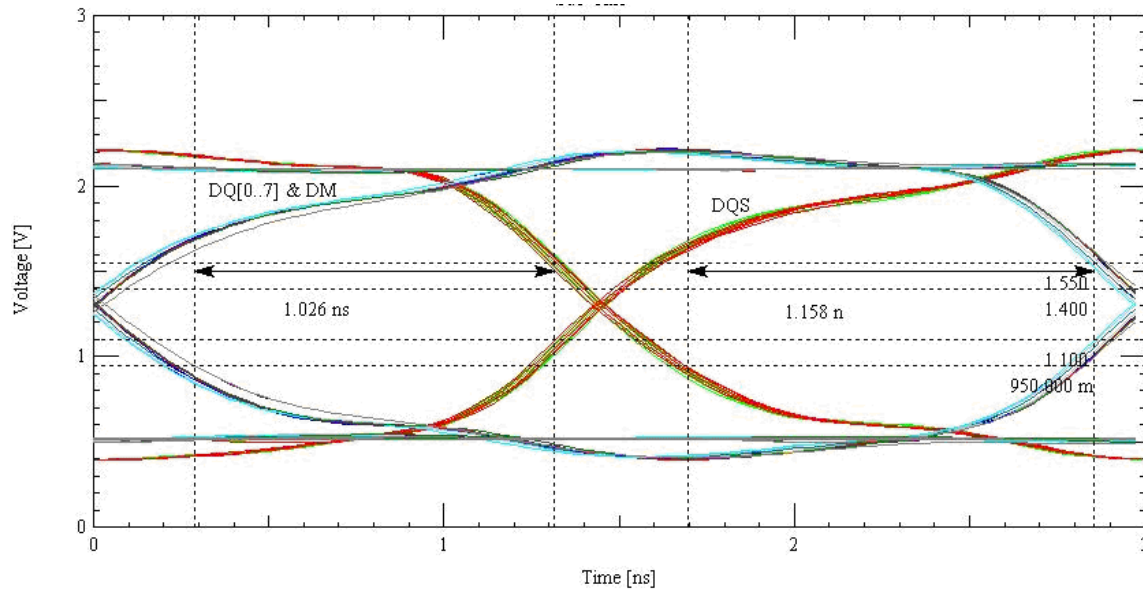
Ground and power planes are drawn so as to provide continuous reference to the data and address signals. Below is the sample power plane of the board





## Post Layout SI Analysis of High Speed PCB

Eye diagram result for single DDR byte along with its strobe is shown below..



### Timing SI Results for DDR section:

The minimum setup and hold timings for CPU1, CPU2 & CPU3 is as follows:

#### For CPU1:

Data group:

Setup time: 1.01ns

Hold time: 1.26ns

Addr/control/command group:

Setup time: 1.318ns

Hold time: 2.018ns

#### For CPU2:

Data group:

Setup time: 1ns

Hold time: 1.31ns

Addr/control/command group:

Setup time: 1.447ns

Hold time: 2.072ns

#### For CPU3:

Data group:

Setup time: 1.01ns

Hold time: 1.28ns

Addr/control/command group:

Setup time: 1.400ns

Hold time: 2.149ns

### The Maximum Peak Crosstalk values are as follows:

For CPU1:146.1mV for the net DDR\_DQ\_11\_50557

For CPU2:146.5mV for the net DDR\_DQ\_28\_89261

For CPU3:156.4mV for the net DDR\_DQ\_2



# Post Layout SI Analysis of High Speed PCB

## PCI section: (66 MHz)

32 bit PCI signals are routed with 50 ohm impedance. Address and Data signals are multiplexed. Post Layout SI and timing analysis is done for the nets of the PCI section (Between CPU and PCI/VME chip) interface. Critical nets of interest for analysis include the 32 Address/Data bits of PCI interface namely PCI\_AD0 to PCI\_AD31 & the PCI clock net PCI\_CLK.

The flight time and clock skew are important parameters in PCI interface operation, so the PCI section signals are verified for positive setup and hold margins. Signals are routed with star topology. The timing report of this section is shown below

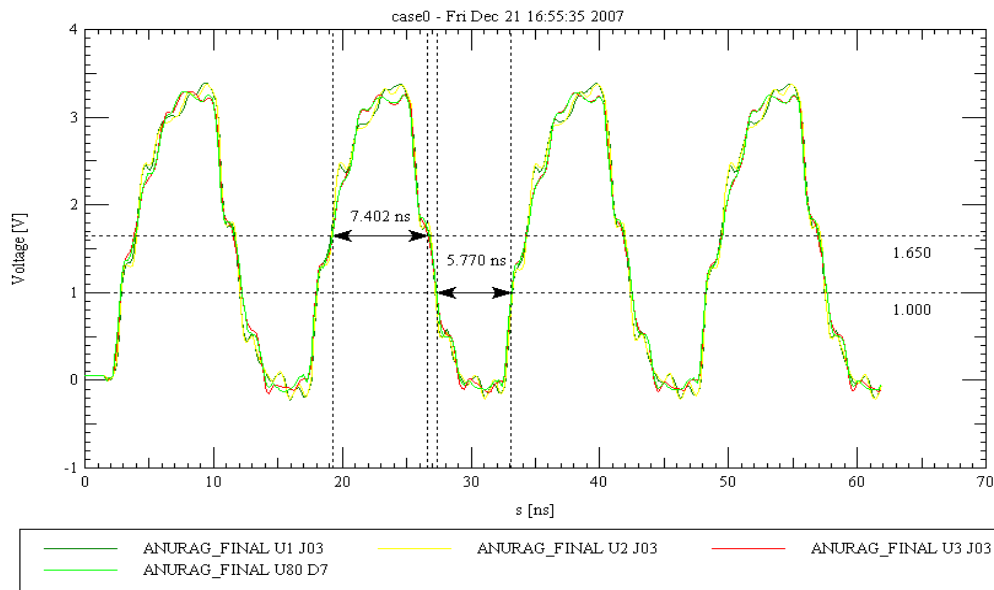
	Min.Setup Margin (ns)	Min.Hold Margin (ns)
CPU1 & PCI	6.711	1.389
CPU2 & PCI	7.209	1.797
CPU3 & PCI	6.116	0.838

## Reflection Analysis

The critical nets PCI\_AD0 to PCI\_AD31 & PCI\_CLK nets of the PCI section (Between CPU and PCI/VME) interface are taken for Reflection Analysis. Below is shown the reflection waveforms taken for PCI Clock net taken at 66 MHz & PCI Address/Data nets.

### Waveform for PCI\_CLK Net

sim1: (ANURAG\_FINAL U2 P02) ANURAG\_FINAL U2 P02 Pulse Typ Reflection





# Post Layout SI Analysis of High Speed PCB

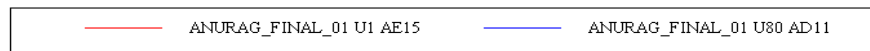
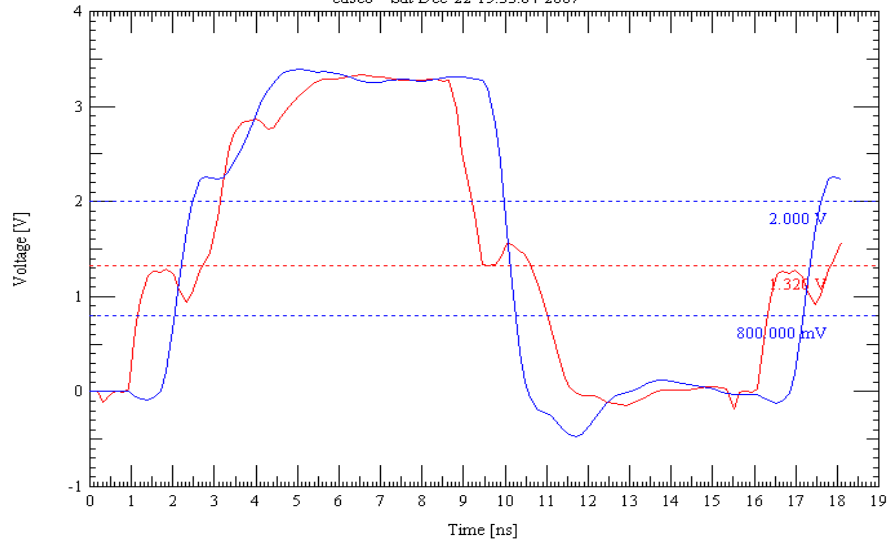
Reflection report when Clock drives CPU1

Driver	Receiver	Cycle	GlitchTol [ns]	FTSMode	Glitch	Monotonic
U2.P02	U1.J03	1	0.0367929	Typ	PASS	PASS
Noise Margin [mV]	Overshoot High [mV]	Overshoot Low [mV]	Prop Delay [ns]	Switch Delay [ns]	Settle Delay [ns]	
603.19	3327.11	-118.78	1.21886	3.0852	4.5337	

## Waveform for PCI\_AD20

JRAG\_FINAL\_01 U1 AE15) ANURAG\_FINAL\_01 U1 AE15 Pulse Typ

case0 - Sat Dec 22 15:33:04 2007



Reflection report when Clock drives CPU1

Driver	Receiver	Cycle	GlitchTol [ns]	FTSMode	Glitch	Monotonic
U1.AE15	U80.AD11	1	0.0367929	Typ	PASS	PASS
Noise Margin [mV]	Overshoot High [mV]	Overshoot Low [mV]	Prop Delay [ns]	Switch Delay [ns]	Settle Delay [ns]	
232.73	3391.46	-475.19	0.66969	2.0407	2.68853	

**The Maximum Peak Crosstalk values for PCI signals are as follows:**

For CPU1:85.23mV for the net PCI\_AD23

For CPU2:130.6mV for the net PCI\_AD4

For CPU3:89.4mV for the net PCI\_AD4



## Post Layout SI Analysis of High Speed PCB

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Flash memory, and power supply components are placed close to the corresponding CPU's. Care has been taken to ensure that sufficient number of vias is placed in the planes according to their current rating requirements.

### **Conclusion**

From the post layout analysis SI and timing, the signal qualities of the critical nets are verified and there is no waveform degradation. This ensures that the high speed effects will be minimized and the board operates at all corners of PVT with good signal integrity.