



Introduction:

In this high speed PCB, the memory controller (CT36106) and DDR DRAM interface is the high speed section which needs analysis and careful planning for good signal integrity. This design document contains the design analysis for the memory controller and DDR DRAM interface. The document contains the following sections:

- Memory interface details.
- Timing and Budget.
- PCB layer stack-up.
- Component Placement.
- Layout Guidelines and Topology.

Controller (CT3616) and DDR DRAM Memory interface:

The memory controller CT3616 from Cradle Technologies supports DDR DRAM up to 1GB in two ranks and specified as DDR -I with SSTL_2 standard logic. The data rate is specified up to 333 MHz. The DDR DRAM from Micron having part number MT46V64M8P-6T:F is selected. The figure 1 shows the interface block diagram and signals flow between controller and DRAM. The DRAM components are organized in two ranks with 8 devices of 512Mb in each rank.

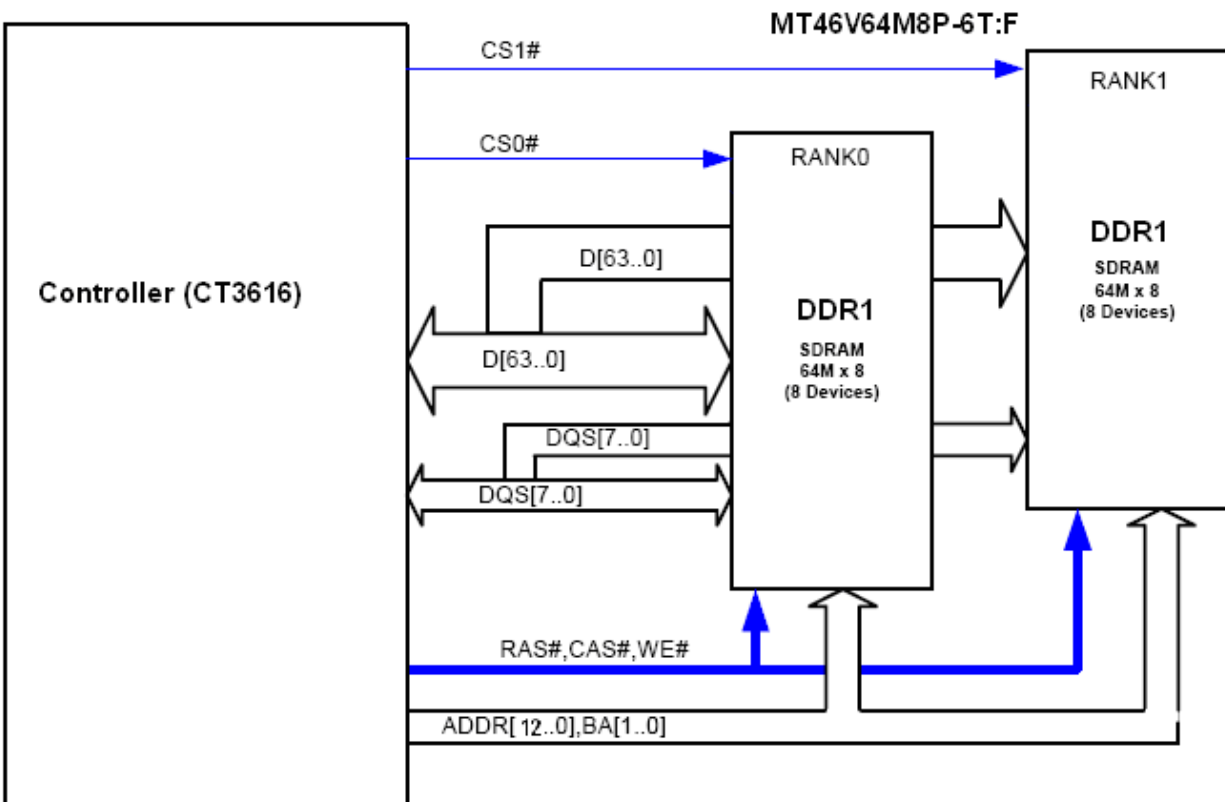


Figure 1: DDR interface Block Diagram



Timing and Budget:

The memory controller and DRAM used in this project is to be operated at 333MHz data rate and the clock is 167MHz. The data transfer is carried out by source synchronous technique. The strobe having clock rate is used to latch the data and the strobe is delayed $\frac{1}{4}$ of clock period with data. The figure 2 shows simple DDR timing waveform diagram. The Address is operated at the clock period and pre launched with $\frac{1}{2}$ of clock period.

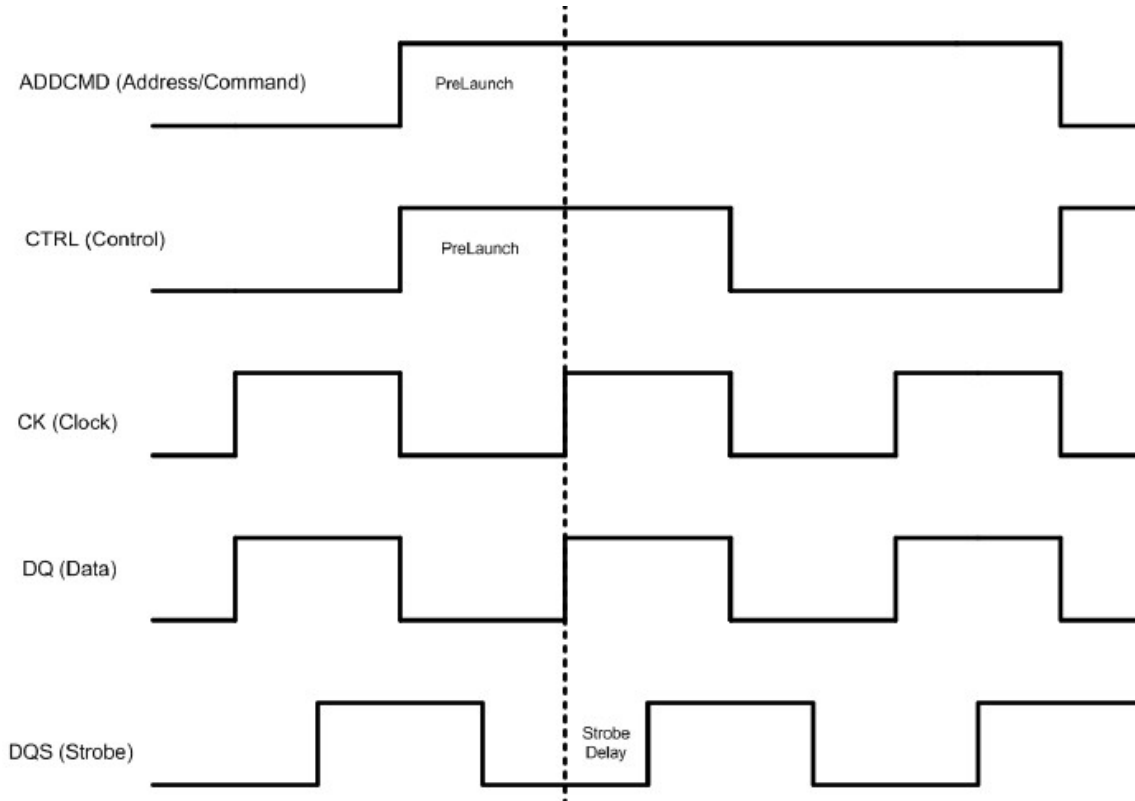


Figure 2: Simple DDR Timing Diagram

The following tables 1, 2 and 3 are showing the timing budget for data write, data read and address. The data and strobe are considered for data write and read budget. The address and clock are considered for address timing budget. The transmitter and memory skew are taken from datasheets of the components. The layout routing tolerance of 100 mil is used for path skew calculation and for propagation delay of 175 ps/inch (dielectric's Er is taken as 4.3), the skew is 17.5 ps. The crosstalk and ISI timing should be verified in post layout analysis for positive margin.



Table 1: DDR Write Budget

ELEMENT	SKEW COMPONENT	SETUP	HOLD	UNITS	COMMENTS
Transmitter (CT3616)	Total Skew at Transmitter	550	550	ps	From data sheet
DRAM device	t _{DH} /t _{DS}	450	450	ps	
MT46V64M8P-6T:F	Total Device	450	450	ps	From data sheet
Interconnect	XTK (cross talk) - DQ	60	60	ps	4 aggressors (a pair on each side of the victim)
	XTK (cross talk) - DQS	30	30	ps	1 shielded victim, 2 aggressors (PRBS)
	ISI - DQ	15	15	ps	
	ISI - DQS	5	5	ps	
	Path Matching	17.5	17.5	ps	Within byte lane: 175 ps/in. × 0.1in. (Er = 4.3)
	Input Capacitance Matching	95	95	ps	4.0pF and 5.0pF loads, strobe and data shift differently
	RTERM VOH/VOL Skew (1%)	20	20	ps	
	Input Eye Reduction (V _{REF})	100	100	ps	±75mV included in DRAM skew; additional = (±25mV)/(.5 V/ns); this includes DQ and DQS
	Strobe-to-Data Skew	10	10	ps	Strobe shifts relative to data (1010 pattern vs. PRBS)
Total Interconnect	Interconnect Skew	352.5	352.5	ps	From simulation
Total Budget	3000/2 @ 333 MHz data rate	1500	1500	ps	
Total Budget Consumed by Controller and DRAM	Transmitter + DRAM	1000	1000	ps	
Interconnect Budget	Total - (transmitter + DRAM)	500	500	ps	Must be greater than amount consumed by board interconnect
Margin		147.5	147.5	ps	

Table 2: Data Read Budget

ELEMENT	SKEW COMPONENT	SETUP	HOLD	UNITS	COMMENTS
DRAM device	Clock 167MHz	6	6	ns	
MT46V64M8P-6T:F	t _{HP} (t _{CL} /t _{CH} [MIN] at 45/55)	2700	2700	ps	
	t _{DQSQ}	450	450	ps	
	t _{QHS}	550	550	ps	
	t _{QH} (t _{HP} - t _{QHS})	2150	2150	ps	
	t _{DV} (t _{HP} - t _{DQSQ} - t _{QHS} , or t _{QH} - t _{DQSQ})	1700	1700	ps	
	(t _{CK} /2 - t _{DV})/2	650	650	ps	
DRAM Total	Total DRAM Data Valid Reduction	650	650	ps	From data sheet
Receiver (CT3616)	Total Skew at Receiver	550	550	ps	From data sheet
Interconnect	XTK (cross talk) - DQ	60	60	ps	4 aggressors (a pair on each side of the victim)
	XTK (cross talk) - DQS	30	30	ps	1 shielded victim, 2 aggressors (PRBS)
	ISI - DQ	50	50	ps	
	ISI - DQS	15	15	ps	
	Path Matching	17.5	17.5	ps	Within byte lane: 175 ps/in. × 0.1in. (Er=4.3)
	RTERM VOH/VOL Skew (1%)	20	20	ps	
	Input Eye Reduction (V _{REF})	100	100	ps	±75mV included in DRAM skew; additional = (±25mV)/(.5 V/ns); this includes DQ and DQS
Total Interconnect	Interconnect Skew	292.5	292.5	ps	From simulation



Total Budget	3000/2 @ 333 MHz data rate	1500	1500	ps	
Total Budget Consumed by Controller and DRAM	Receiver + DRAM	1200	1200	ps	
Interconnect Budget	Total - (Receiver + DRAM)	300	300	ps	Must be greater than amount consumed by board interconnect
Margin		7.5	7.5	ps	

Table 3: Address Timing Budget

ELEMENT	SKEW COMPONENT	SETUP	HOLD	UNITS	COMMENTS
Transmitter (CT3616)	Total Skew at Transmitter	550	550	ps	From data sheet
DRAM device	tIS, tIH	800	800	ps	tIS, tIH from DRAM spec (slow edge). tIS: additional 50ps for every 0.1 V/ns below 0.5 V/ns (0.3 V/ns)
MT46V64M8P-6T:F	Total Device	800	800	ps	From data sheet
Interconnect	Cross Talk - Address	640	640	ps	1 shielded victim, 4 aggressors (PRBS)
	ISI - Address	690	690	ps	(PRBS)
	Cross Talk - Clock	25	25	ps	Spec.
	VREF: Reduction	50	50	ps	$\pm 75\text{mV}$ included in DRAM skew; additional = $(\pm 25\text{mV}) / (.5 \text{ V/ns})$
	Path Matching	17.5	17.5	ps	Within byte lane: $175 \text{ ps/in.} \times 0.1 \text{ in.} (Er=4.3)$
	Input Capacitance Matching	105	105	ps	1.5pF for 5 device, 2.5pF for 18 device (1610-1400) = 210 total
	Compensating Capacitor Skew (5%)	60	60	ps	Compensating capacitor 5% tolerance
	RTERM VOH/VOL Skew (1%)	10	10	ps	Estimator Tool
Total Interconnect	Interconnect Skew	1597.5	1597.5	ps	From simulation
Total Budget	6000/2 @ 333 MHz data rate	3000	3000	ps	
Total Budget Consumed by Controller and DRAM	Transmitter + DRAM	1350	1350	ps	
Interconnect Budget	Total - (transmitter + DRAM)	1650	1650	ps	Must be greater than amount consumed by board interconnect
Margin		52.5	52.5	ps	

PCB layer stack-up:

The 12 layer PCB stack-up is selected and shown in table 4. The dielectric material FR4 with $E_r = 4.3$ is selected. The characteristic impedance for single ended signals of memory interface is 60 ohm and the differential impedance for clock is 120 ohm. The PCB thickness should be 63 mil +/- 8mil in the guide area (100mil from board edge).



Table 4: PCB layer stack-up

12 layers	Thickness inch	Z0(w=4mil) ohm	Z0(w=5mil) ohm	Zdiff(w=4&12mil spacing)	Routing Plan
SM	0.001				
T	0.0014	59.2	54.1		
Er=4.3	0.004				
G	0.0007				
Er=4.3	0.007				
S1	0.0007	58.8	52.2	113.3	DDR DATA BUS and CLOCK
Er=4.3	0.007				
G	0.0007				
Er=4.3	0.007				
S2	0.0007	58.8	52.2	113.3	DDR ADDRESS, CTRL and CMD
Er=4.3	0.007				
P	0.0014				
	0.003				
G	0.0014				
Er=4.3	0.007				
S3	0.0007	58.8	52.2	113.3	DDR DATA BUS and CLOCK
Er=4.3	0.007				
G	0.0007				
Er=4.3	0.007				
S4	0.0007	58.8	52.2	113.3	DDR ADDRESS, CTRL and CMD
Er=4.3	0.007				
P	0.0007				
Er=4.3	0.004				
B	0.0014	59.2	54.1		
SM	0.001				
Total	0.0802				

Component Placement:

Figure 3 shows the controller and DRAM components placement plan. As the DRAM is in TSOP package, it can be placed Top and Bottom of the PCB board. The 8 DRAM components are to be placed in top (rank 0) and the other 8 DRAM components in the bottom (rank 1). The VTT Island and components are to be placed at the end after the DRAM. The VTT Island and regulator placement is shown in the figure 4. The bulk capacitors are to be placed at the ends of the VTT Island.

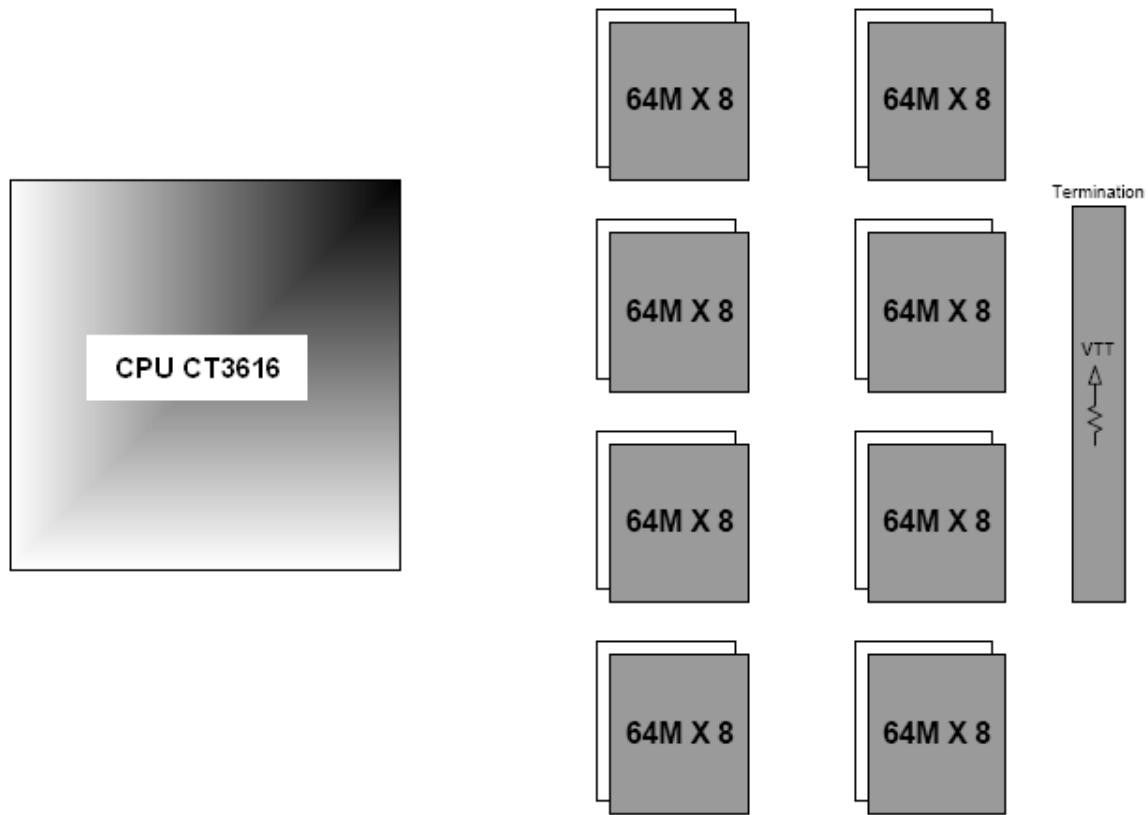


Figure 3: CPU and DRAM Placement (Top – “Rank 0” and Bottom – “Rank 1”)

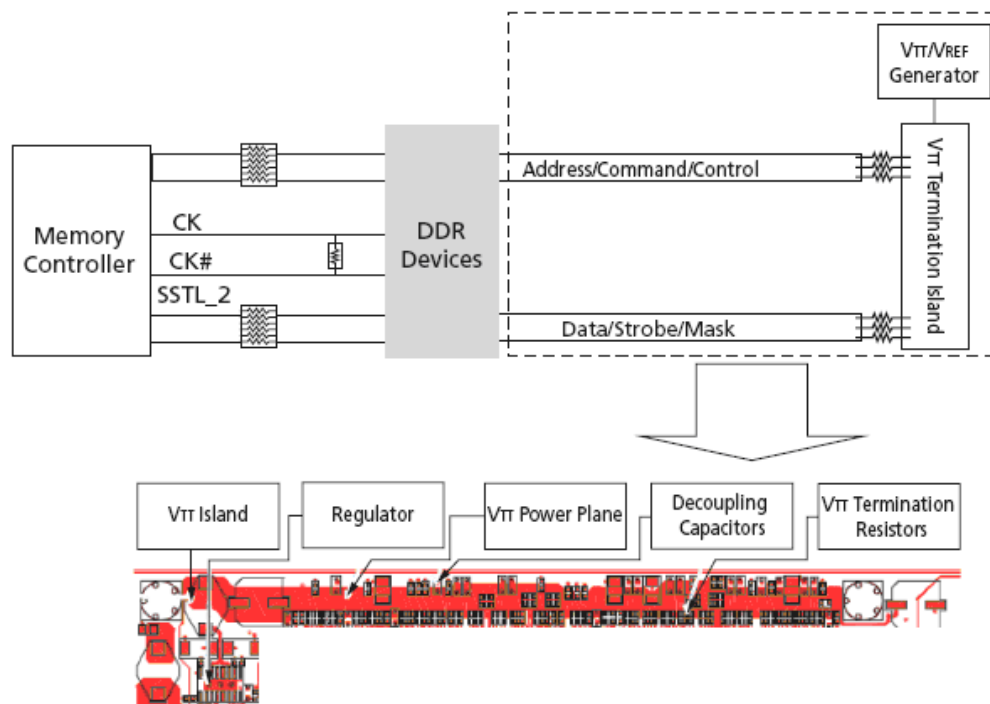




Figure 4: VTT Island and Regulator layout for Multiple DDR Components.

Layout Guidelines and Topology:

The following are the routing guidelines for the DDR memory interface section:

1. Single ended trace's controlled impedance $Z_0 = 60$ ohm.
2. DQ, strobe, and clock signals are referenced to VSS, while address, command, and control signals can be referenced to VDD.
3. Address, command, and control signals length are matched to clock with +/- 100 mil.
4. $DQ<0..7>$ & DM signals length are matched to corresponding DQS with +/- 100 mil (byte lane).
5. One byte lane traces should be routed on same layer.
6. Byte lane to byte lane is matched to clock with +/- 500 mil.
7. CK&CK# are matched with +/- 30 mil and routed as diff pair with 120ohm differential impedance.
8. Clock Pair to pair matching tolerance is +/- 30 mil.
9. Trace to trace spacing is 2X and signal group to group is 3X.
10. Route DQS middle of the byte lane ($DQ<0..7>$).
11. Clock trace split point to DRAM should be < 1 inch.
12. VTT and VREF islands must be separated by a minimum of 150.
13. VTT island surface trace width = 150 mil min.; 250 mil preferred.
14. Route VREF with a 20–25 mil minimum trace

The figure 5 shows the data bus topology and figure 6 shows the address/control bus topology. The clock trace is to be routed as differential pair. The CLK1 is routed to 6 DRAM components (Top-3 & Bottom-3), CLK2 to 6 DRAM components (Top-3 & Bottom-3) and CLK3 to 4 DRAM (Top-2 & Bottom-2). The split point of the clock should be parallel terminated with 120 ohm.

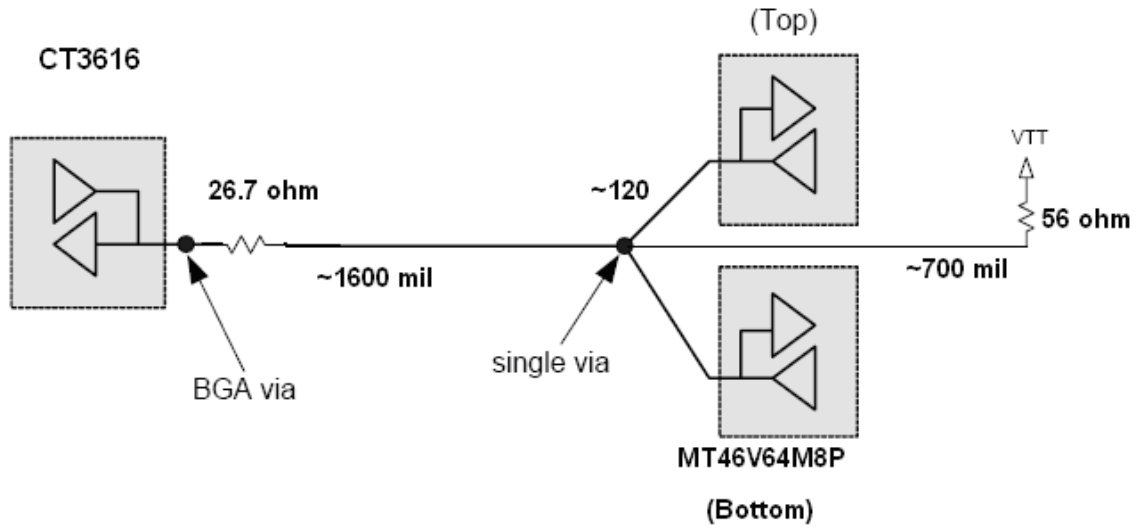


Figure 5: Data bus topology

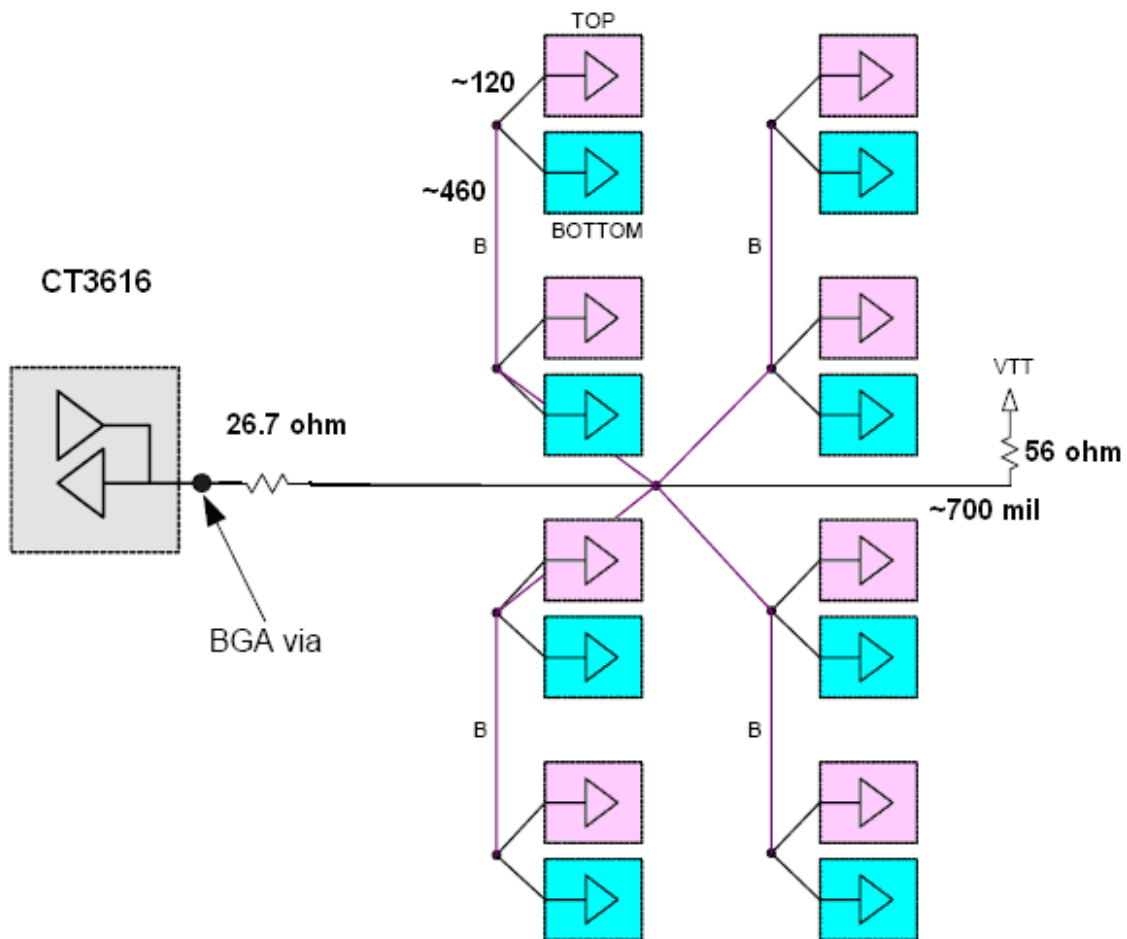


Figure 6: Address and Control bus Topology

**Conclusion:**

The memory controller and DDR DRAM interface design analysis and timing budget is described. The component placement, PCB layer stack-up, routing guidelines and topology are suggested for good signal integrity. The post layout analysis is to be carried out to ensure the crosstalk and ISI timing budget requirement. Also, the reflection and ringing are to be studied for good impedance matching in the interface in post layout analysis.

Reference:

1CT3616 Data book from Cradle Technologies

2MT46V64M8P-6T:F datasheet from Micron

3TN-46-14: Hardware Tips for Point-to-Point System Design from Micron

4TN-46-07: DDR333 Design Guide for Two-DIMM Systems from Micron