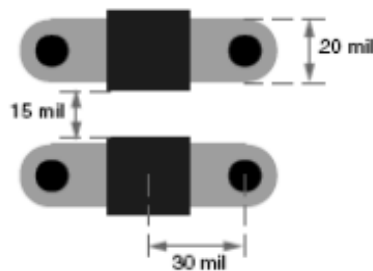




## 1. Optimum Power Rails

- ◆ To ensure low inductance and low IR-Drop in power net, the power net should have high track width (200 mil).
- ◆ The full power plane with high parasitic capacitance needs to be avoided.
- ◆ The De-caps need to be connected using short via with good strategy to reduce the via inductance and also to reduce SSN as shown below:

0402 Land Pattern, double side vias, 0.4nH



- ◆ Use surface mount capacitors to minimise the lead inductance.
- ◆ Use large diameter vias.
- ◆ Don't share vias with adjacent capacitor.
- ◆ Place power and ground planes close to the surface where the capacitors are attached.
- ◆ Short length of power/Ground nets is essential for reduced IR-Drop.

## 2. Impedance and length Matching

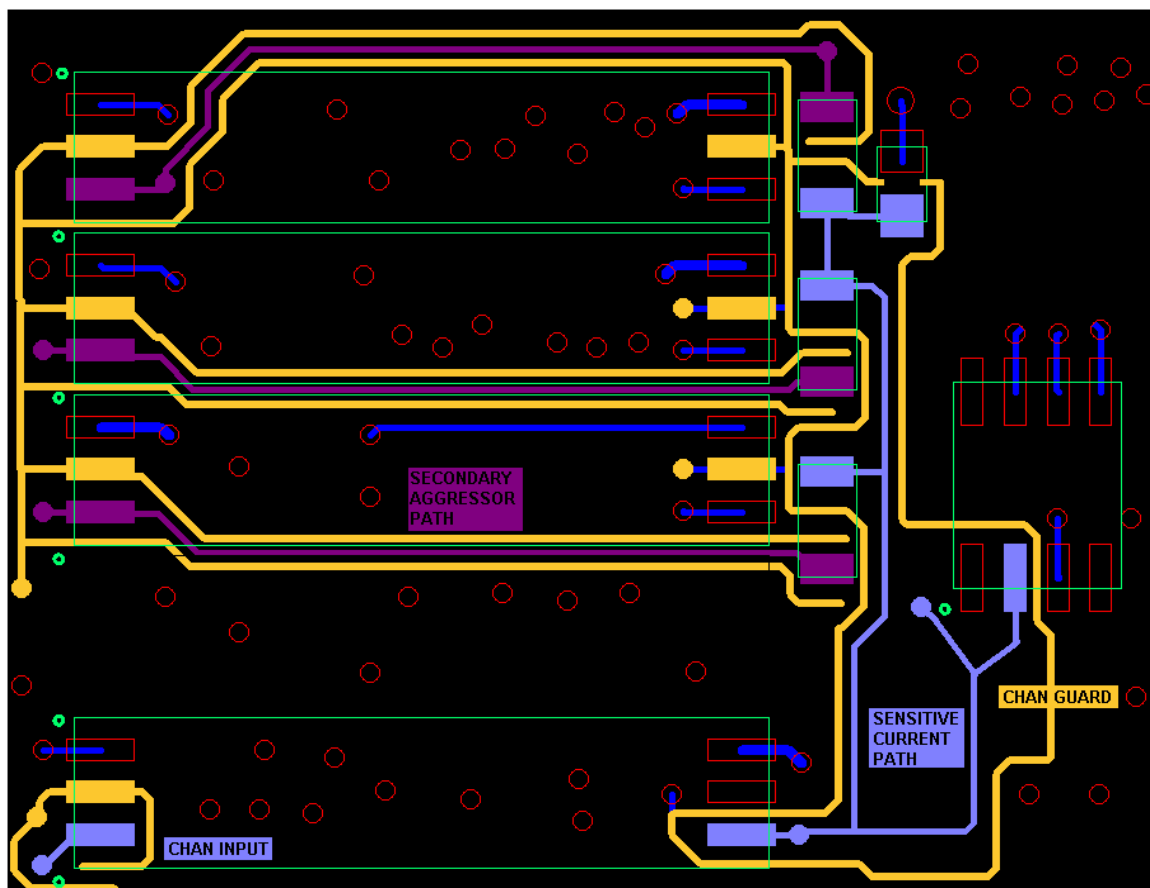
- ◆ To avoid the signal loss and make sure the reflection free signals, all the traces should be impedance matched between source and DUT sides.
- ◆ To avoid the differential to common mode noise generation and energy loss, all the differential pairs should be routed as differential pairs with length matched between individual traces .
- ◆ To avoid correlation issues, the critical traces and placement should be identical across all the sites in multi-site testing.



### 3. Reduction of Leakage Current

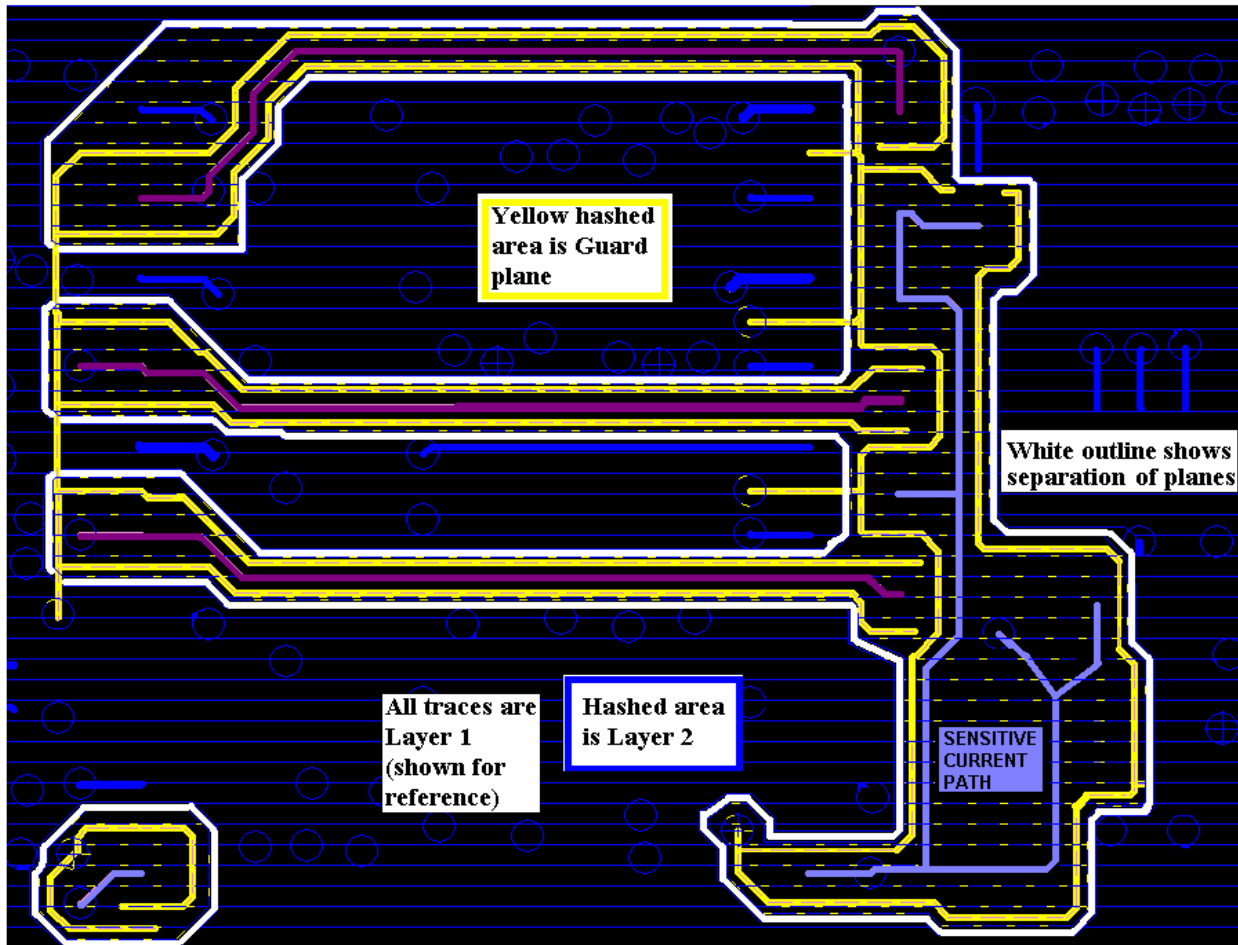
- ◆ To reduce leakage current, the low loss dielectric material like Rogers or Teflon can be used.
- ◆ The dielectric thickness can be 6 mil minimum to reduce the leakage between power and ground plane.
- ◆ The signal routing can have guarding to reduce any noise coupling from nearby signals as given below (The yellow tracks are guard):

Top Layer





### Inner Layer





### Vias and Inner Traces on Subsequent Layers

